ALL SHORE INDUSTRIES

ASI-T-9204619A10MPN/D

Item	Contents	Unit
Size	9.2	inch
Resolution	462 (RGB) x 1920	/
Interface	MIPI	/
Technology type	IPS TFT	/
Pixel Configuration	R.G.B. Stripe	
Pixel pitch	0.1178 x 0.1178	
Outline Dimension (W x H x D)	242.25 x 61.64 x 4.61	mm
Active Area	226.25 x 54.44	mm
Display Mode	Transmissive, Normally Black	/
Display Driver IC	FL7707N	/
Backlight Type	LED	/
Viewing Direction	ALL	/

Record of Revision

Date	Revision No.	Summary
2023-07-17	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of ASI-T-9204619A10MPN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 9.2” display area contains 462(RGB) x 1920 pixels.

As to basic specification of the driver IC, refer to the IC specification and datasheet.

2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

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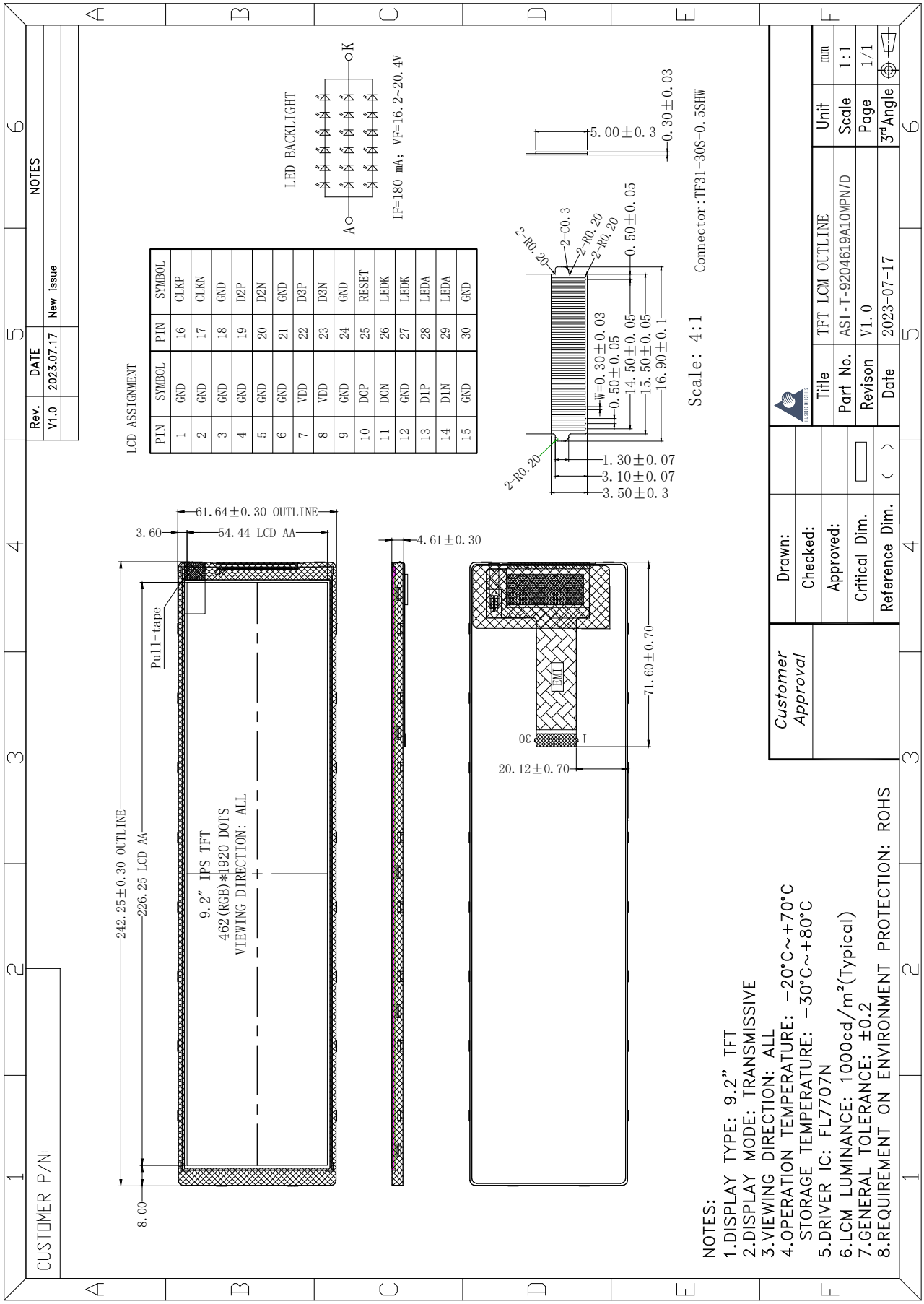
Backlight Type	LED	/
Viewing Direction	ALL	/

4. Outline Drawing



5. Interface signals

No	Symbol	Description	Remark
1~6	GND	Power ground	
7~8	VDD	Power supply for analog circuit	
9	GND	Power ground	
10	D0P	MIPI data input Lane0 positive-end	
11	D0N	MIPI data input Lane0 negative-end	
12	GND	Power ground	
13	D1P	MIPI data input Lane1 positive-end	
14	D1N	MIPI data input Lane1 negative-end	
15	GND	Power ground	
16	CLKP	MIPI clock input positive-end	
17	CLKN	MIPI clock input negative-end	
18	GND	Power ground	
19	D2P	MIPI data input Lane2 positive-end	
20	D2N	MIPI data input Lane2 negative-end	
21	GND	Power ground	
22	D3P	MIPI data input Lane3 positive-end	
23	D3N	MIPI data input Lane3 negative-end	
24	GND	Power ground	
25	RESET	Reset pin	
26~27	LEDK	LED backlight cathode	
28~29	LEDA	LED backlight anode	
30	GND	Power ground	

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	VDD	-0.3	3.6	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VDD	2.5	3.3	3.6	V	
Input signal voltage	H level	V_{IH}	0.7*VDD	-	VDD	V	
	L level	V_{IL}	GND	-	0.3*VDD	V	
Current of Power Supply		ILCD	-	90	135	mA	VDD=3.3V

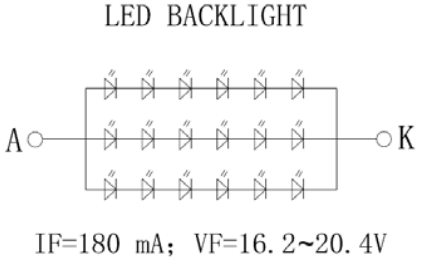
7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IL	-	180	-	mA	
Forward Voltage	VL	16.2	-	20.4	V	Note1
LED life time	--	30,000	-	-	Hr	Note2

Notes:

1. The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IL =180mA.
2. The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=180mA. The LED lifetime could be decreased if operating IL is larger than 180mA.



8. Command/AC Timing

8.1 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI stand builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The FL7707N only support Video mode.

Video mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the driver IC relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Lane Pair	HOST(Master)/ Driver IC(Slave)
Clock Lane	- Unidirectional Lane - Clock Only - Escape mode (ULPS only)
Data Lane 0	- Bi-directional Lane - Forward High Speed - Bi-directional Escape Mode - Bi-directional LPDT
Data Lane 1 Data Lane 2 Data Lane 3	- Unidirectional Lane - Forward High Speed - Escape mode (ULPS only) - NO LPDT

Tabel: MIPI Interface Configuration

8.2 DSI General Interface Communication

The driver IC uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the HOST to the driver IC and vice versa.

State code	Line voltage Levels		High speed	Low power	
	DP	DN		Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	Note 1	Note 1
HS-1	HS High	HS Low	Differential-1	Note 1	Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note 2

Table: Lane State Description

Notes:
1. During high-speed transmission, the low power receivers observe LP-00 on the lines.
2. If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11)

8.3 DSI Clock Lane

The principle flow chart of the different clock lanes power modes is illustrated below.

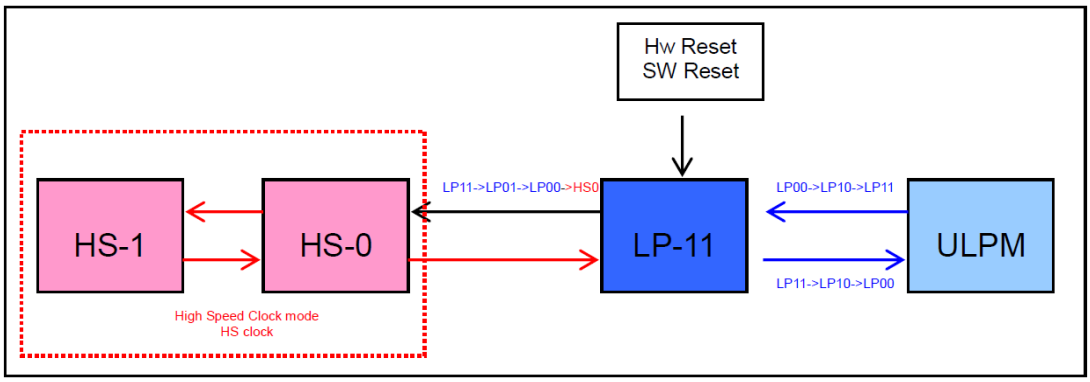


Figure: DSI Clock Lane State Diagram

Low Power Mode (LP-11: Stop)
DSI-C

LK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11:
1. After SW Reset, HW Reset or Power On Sequence =>LP-11
2. After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00) =>LP-10=>LP-11 (LPM).
This sequence is illustrated below.

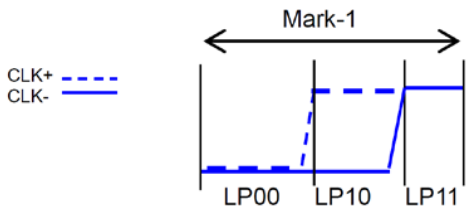


Figure: From ULPM to LPM

3. After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.

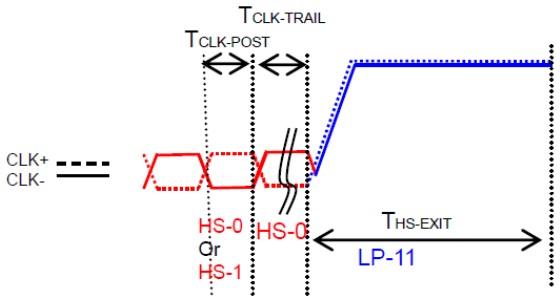


Figure: From High Speed Clock mode to LPM

Ultra Low Power Mode (LP-00: ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State. The entering way is from the Low Power Mode (LPM, LP-11 State) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.

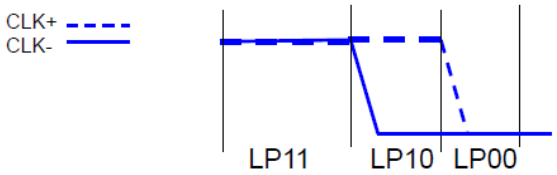


Figure: From LPM mode to ULPM

8.4 DSI-D0 Data Lane

DSI-D0+/- Data Lanes can be driven in different modes which are: Escape Mode, High-Speed Data Transmission and Bus Turnaround Request. The flow chart of the D0 data lanes is illustrated below.

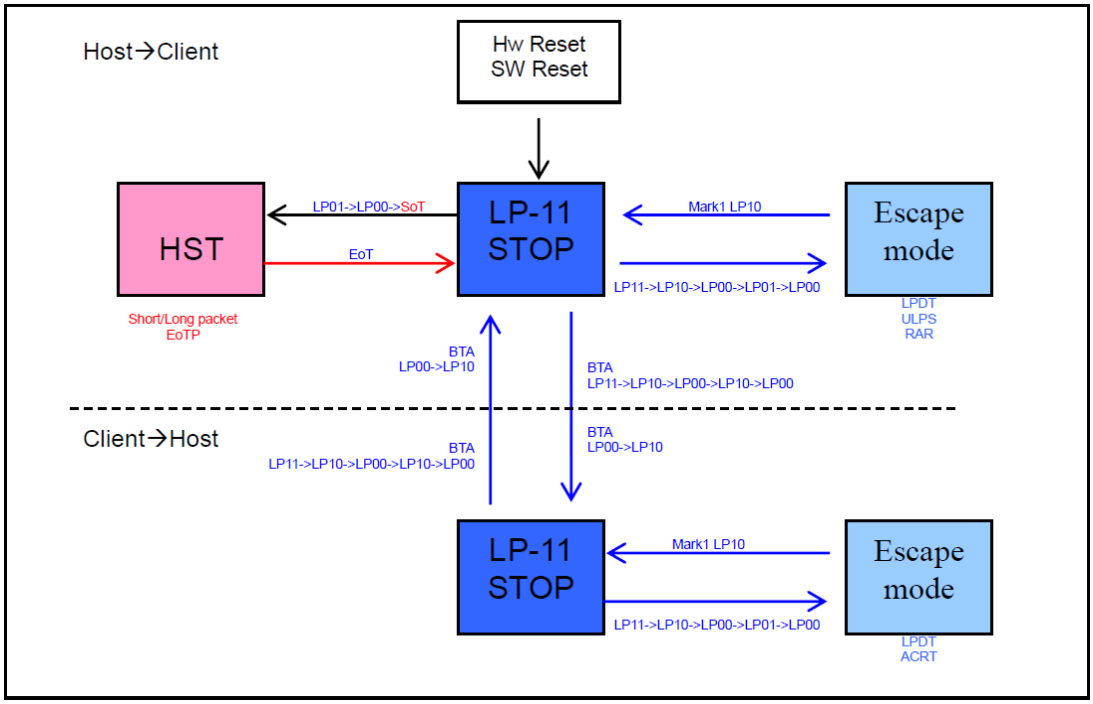


Figure: DSI Data Lane D0 State Diagram

Description	Operation Code
High Speed Data Transmission Burst	LP11->LP01->LP00
Escape mode entry	LP11->LP10->LP00->LP01->LP00
Bus turn around	LP11->LP10->LP00->LP10->LP00
Exit Escape mode (Mark-1)	LP00->LP10->LP11

Table: Data Lane D0 Operation Modes

ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

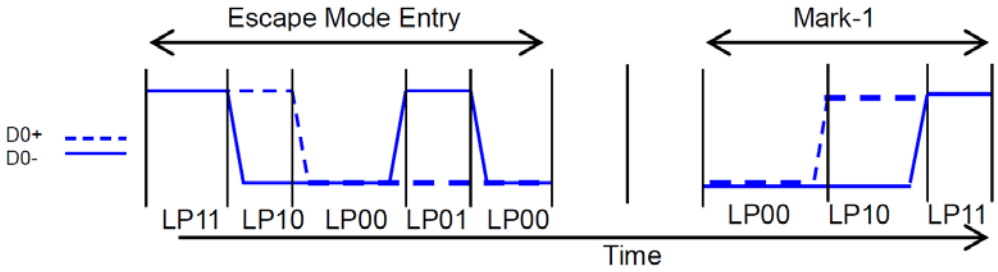


Figure: DSI Data Lane D0 general escape mode sequence

FL7707N can support three different Escape Commands. The commands (EC) can be divided 2 different groups: Mode or Trigger. The HOST is informing to the driver IC that it is controlling data lanes (DSI-D0+/-) with the mode. Escape commands are defined as below table.

Escape Command	Command Type	Entry Command Pattern (First Bit→Last Bit Transmitted)
Low Power Data Transmission	Mode	1110 0001
Ultra-Low Power mode	Mode	0001 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001

Table: Escape Mode Commands

Low-Power Data Transmission (LPDT)

The HOST can send data to the driver IC in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command will been sent to this driver IC. The driver IC is also using the same sequence when it is sending data to the HOST. The Low Power Data Transmission (LPDT) is using a following sequence:

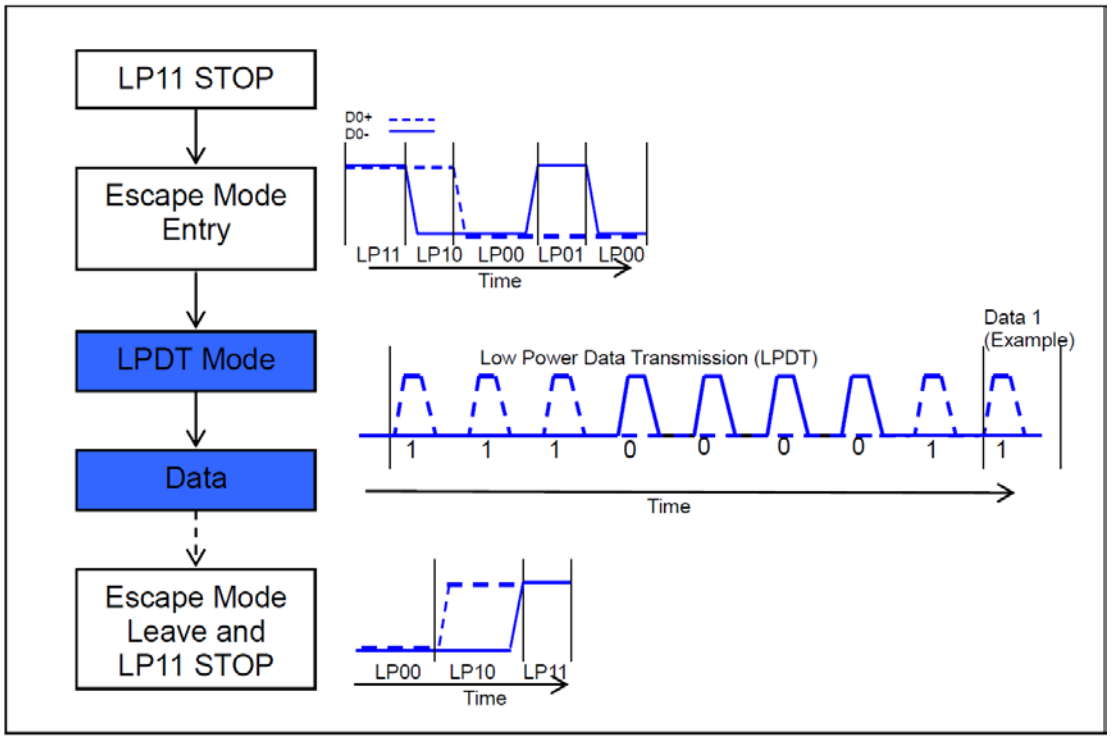


Figure: DSI Data Lane D0 LPDT sequence

9. Optical Specification

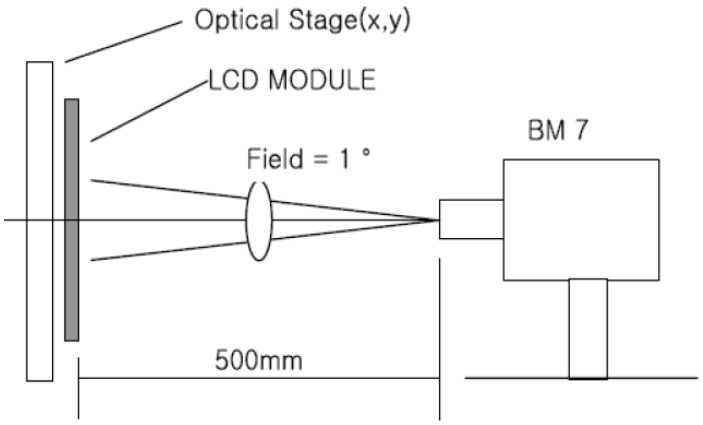
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	800	1000	-		Note1 Note2
Response Time		Tr+Tf	25℃	-	30	35	ms	Note1 Note3
View Angles		ΘT	CR≧10	80	85	-	Degree	Note 4
		ΘB		80	85	-		
		ΘL		80	85	-		
		ΘR		80	85	-		
Chromaticity	White	x	Brightness is on	Typ-0.05	0.2730	Typ+0.05		Note5, Note1
		y			0.3177			
	Red	x			0.6336			
		y			0.3562			
	Green	x			0.3154			
		y			0.5976			
	Blue	x			0.1377			
		y			0.1139			
Luminance		L		-	1000	-	cd/m2	Note1 Note6
Uniformity		U		80	-	-	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

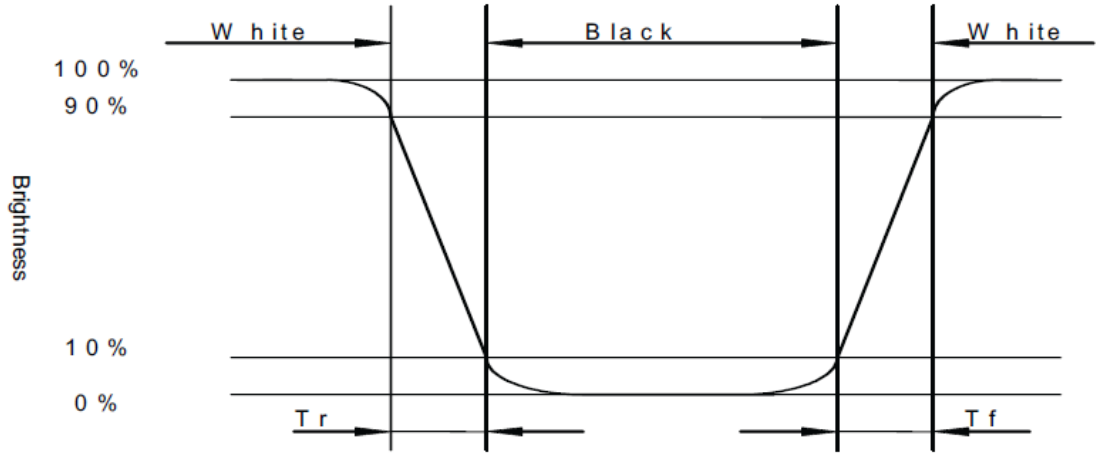


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

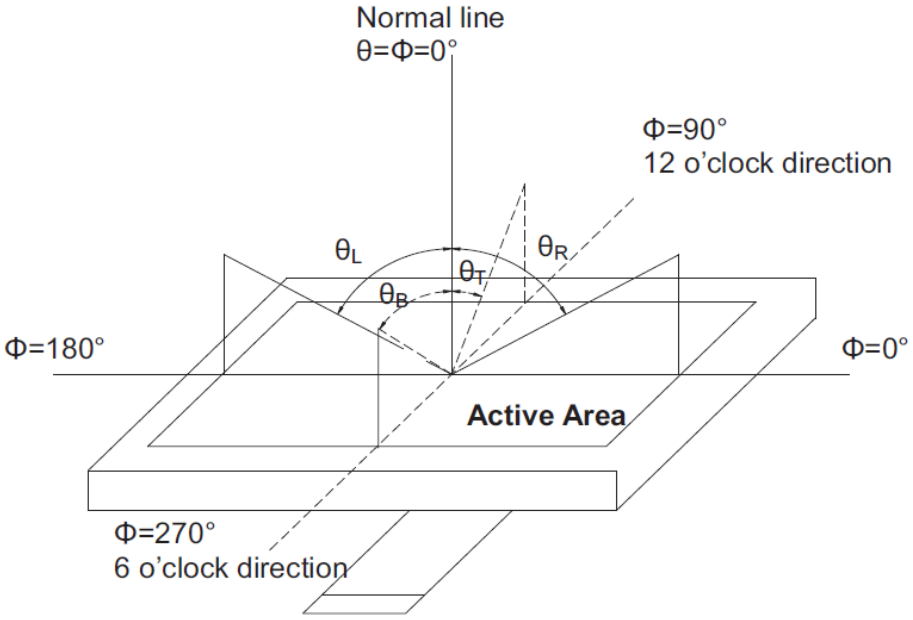
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



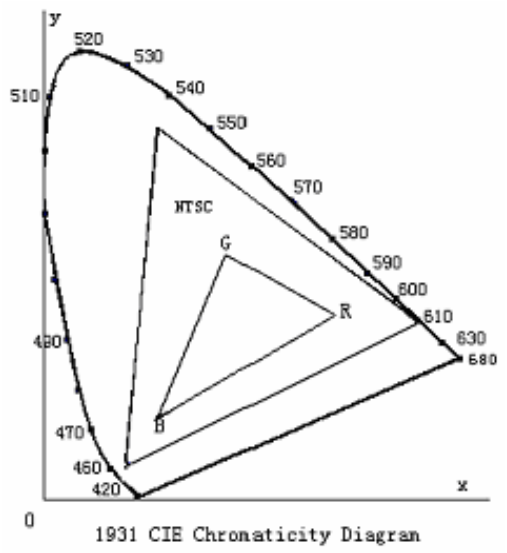
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

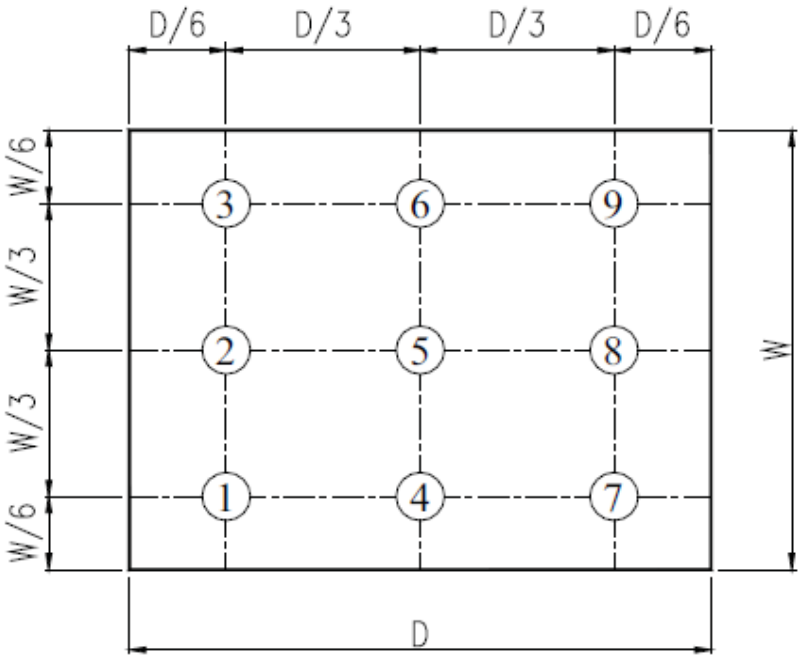


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta= +70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta= -20℃, 120hrs	Per table in below
3	High Temp Storage	Ts= +80℃, 120hrs	Per table in below
4	Low Temp Storage	Ts= -30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ts= +40℃, 90% RH, 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+80℃ 30 min, Change time:5min, 5Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω， 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11.Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press th touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, ASI recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.