ALL SHORE INDUSTRIES

ASI-T-7002814A3MPN/D

Item	Contents	Unit
Size	7.0	inch
Resolution	280(RGB) x 1424	/
Interface	MIPI	/
Technology type	IPS TFT	/
Pixel Configuration	R.G.B. Stripe	
Pixel Pitch	0.12 x 0.12	
Outline Dimension (W x H x D)	38.20 x 181.47 x 3.40	mm
Active Area	33.60 x 170.88	mm
Display Mode	Transmissive, Normally Black	/
Backlight Type	LED	/
Driver IC	OTA7290B	/
Viewing Direction	ALL	/

Record of Revision

Date	Revision No.	Summary
2021-12-03	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of ASI-T-7002814A3MPN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 7.0" display area contains 280(RGB) x 1424 pixels.
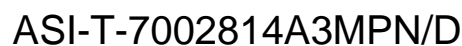
As to basic specification of the driver IC, refer to the IC specification and datasheet.

2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

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4. Outline Drawing

Pin assignment table:

Pin NO.	Symbol
1	GND
2	D0P
3	D0N
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16~17	GND
18~19	NC
20	REFCLK/NC
21	SDA /NC
22	SCL /NC
23	IRQ
24	RESET
25	STBYB/NC
26	NC
27	GND
28~29	K
30	GND
31	NC
32~33	GND
34	NC
35~36	A
37	GND
38	VDD 3.3V
39	VDD 3.3V
40	NC

NOTES revision table:

Rev.	DATE	NOTES
V1.0	2021.12.03	New issue

LED CIRCUIT DIAGRAM:

8EA   If=40mA Vf=24V(Typ)

DETAIL A (4:1)

3.5±0.3
0.3±0.03
W=0.3±0.03
P0.5*(40-1)=19.5±0.05
20.5±0.1
0.5±0.1
2.2-0R-2.7

5.0±0.5

BACK
FRONT
CONTACT SIDE
STIFFNENR PI
0.30±0.05
3.40
2.00 Max.

Pull-tape
1.30
2.30
38.20±0.30 BL
35.60 LCD
33.60 AA
(19.10)
7.0" IPS
280(RGB)X1424
(87.54)
2.10
170.88 AA
0.90
179.70 LCD
181.47±0.30 BL
8.85±0.50
50.00±0.50

DETAIL A

NOTES:
1.DISPLAY TYPE: 7.0" TFT
2.DISPLAY MODE: TRANSMISSIVE, Normally Black
3.VIEW DIRECTION: ALL
4.OPERATION TEMPERATURE: -20°C~+70°C
   STORAGE TEMPERATURE: -30°C~+80°C
5.DRIVER IC: OTA7290B
6.LCM LUMINANCE: 300cd/m² (Typical)
7.GENERAL TOLERANCE: ±0.2
8.REQUIREMENT ON ENVIRONMENT PROTECTION: ROHS

CUSTOMER P/N:

Customer Approval

Drawn:
Checked:
Approved:
Critical Dim.
Reference Dim.

Title	TFT LCM OUTLINE		Unit	mm
Part No.	ASI-T-7002814A3MPN/D		Scale	1:1
Revison	V1.0		Page	1/1
Date	2021-12-03		3rd Angle	

5. Interface signals

5.1 LCM Pin Definition

No	Symbol	Description	Remark
1	GND	Ground	
2	D0P	Positive polarity of low voltage differential data signal (Data lane 0)	
3	D0N	Negative polarity of low voltage differential data signal (Data lane 0)	
4	GND	Ground	
5	D1P	Positive polarity of low voltage differential data signal (Data lane 1)	
6	D1N	Negative polarity of low voltage differential data signal (Data lane 1)	
7	GND	Ground	
8	CLKP	Positive polarity of low voltage differential clock signal	
9	CLKN	Negative polarity of low voltage differential clock signal	
10	GND	Ground	
11	D2P	Positive polarity of low voltage differential data signal (Data lane 2)	
12	D2N	Negative polarity of low voltage differential data signal (Data lane 2)	
13	GND	Ground	
14	D3P	Positive polarity of low voltage differential data signal (Data lane 3)	
15	D3N	Negative polarity of low voltage differential data signal (Data lane 3)	
16~17	GND	Ground	
18~19	NC	No connection	
20	REFCLK/NC	No connection	
21	SDA/NC	Serial in/out signal pin/No connection	
22	SCL/NC	Serial interface clock pin/No connection	
23	IRQ	No connection	
24	RESET	Global reset signal input pin	
25	STBYB/NC	Standby mode control pin/No connection	
26	NC	No connection	
27	GND	Ground	
28~29	K	LED backlight cathode	
30	GND	Ground	
31	NC	No connection	
32~33	GND	Ground	
34	NC	No connection	
35~36	A	LED backlight anode	

37	GND	Ground	
38~39	VDD 3.3V	Power supply voltage	
40	NC	No connection	

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	VDD	-0.5	4.0	V	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. VCC >GND must be maintained.
3. Please be sure users are grounded when handing LCD Module.

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

Notes:

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature. The phenomenon is reversible.
3. Ta<=40℃:85%RH MAX.

    Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power supply voltage	VDD	2.7	3.3	3.6	V	Note 1
Input logic high voltage	V_{IH}	0.7*VDD	-	VDD	V	
Input logic low voltage	V_{IL}	0	-	0.3*VDD	V	

7.2 LED Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Voltage for LED backlight	VL	-	24	-	V	Note 1
Current for LED backlight	IL	-	40	-	mA	
LED life time	-	-	30,000	-	Hrs	Note 2

Notes:

1. The LED Supply Voltage is defined by the number of LED at Ta=25℃ and IL =40mA.

2. The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL =40mA. The LED lifetime could be decreased if operating IL is larger than 40mA.

LED CIRCUIT DIAGRAM:

A ○—▶|▶|▶|▶|▶|▶|▶|▶|—○ K
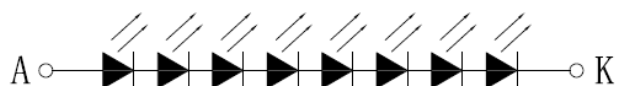
8EA   If=40mA Vf=24V(Typ)

8. Command/AC Timing

8.1 AC Electrical Characteristics

8.1.1 HS Receiver AC Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Bandwidth per lane	-	-	-	1000	Mbps	Note 1
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI_{INST}	1	-	12.5	ns	Note 2
Data to clock skew	tskew	-0.15	-	0.15	UI_{INST}	
Inter-lane static skew	tskew-lane	-	-	UI_{INST} /50	UI_{INST}	
Data to clock setup time	T_{SETUP}	0.25	-	-	UI_{INST}	Note 3
Data to clock hold time	T_{HOLD}	0.25	-	-	UI_{INST}	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	Note 5
Common-mode interference 50MHz- 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	Note 4, 7
Common-mode termination	C_{CM}	-	-	60	pF	Note 6

Notes:

1. Bandwidth selected by register 'speedup'

    Speedup=0 → Max=550Mbps

    Speedup=1 → Max=1000Mbps

2. Total silicon and package delay budget of 0.3*UINST

3. Total setup and hold window for receiver of 0.3*UINST

4. Excluding 'static' ground shift of 50mV

5. =VCMRX (HF) is the peak amplitude of a sine wave superimposed on the receiver input

6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

7. Voltage difference compared to the DC average common-mode potential.
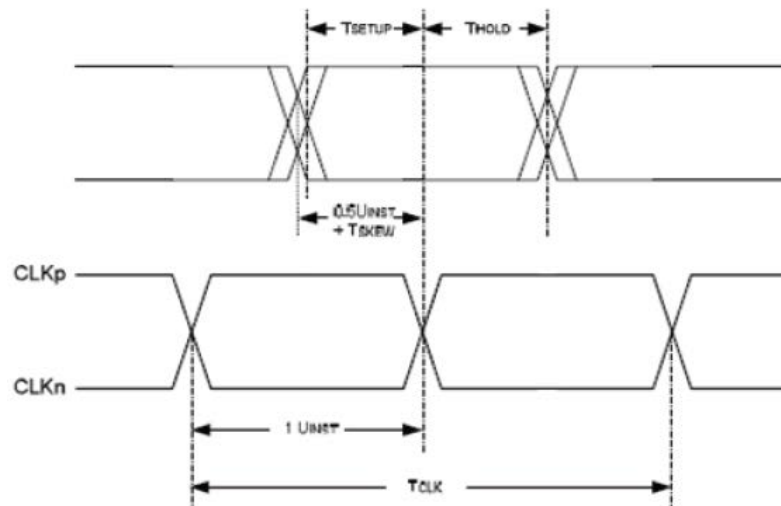
8.1.2 LP Receiver AC Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Input pulse rejection	e_{SPIKE}	-	-	300	Vps	Note1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic o input voltage Not in ULP state	V_{IL}	-	-	550	mV	
Logic o input voltage ULP state	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

Notes:

1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1state.

2. An impulse less than this will not change the receiver state.

3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

8.2 DC Characteristics

8.2.1 HS Receiver DC Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operation voltage	VDD	1.5-10%	1.5	1.5+10%	mV
Differential input voltage	IVIDI	70	200	260	mV
Common mode voltage	$V_{CMPR(DC)}$	70	-	330	mV
Differential input high threshold voltage	VTH	-	-	70	mV
Differential input low threshold voltage	VTL	-70	-	-	mV
Singled-ended input high voltage	V_{IHHS}	-	-	460	mV
Singled-ended input low voltage	V_{ILHS}	-40	-	-	mV
Singled-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
Pin leakage current	I_{LEAK}	-10	-	10	uA
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV
Common-mode interference 50MHz-450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV
Common-mode termination	C_{CM}	-	-	60	pF
Embedded termination	R_T	90	100	110	ohm

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

8.2.2 LP Receiver DC Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage, not in ULP state	V_{IL}	-	-	550	mV
Input hysteresis	V_{HYST}	25	-	-	mV
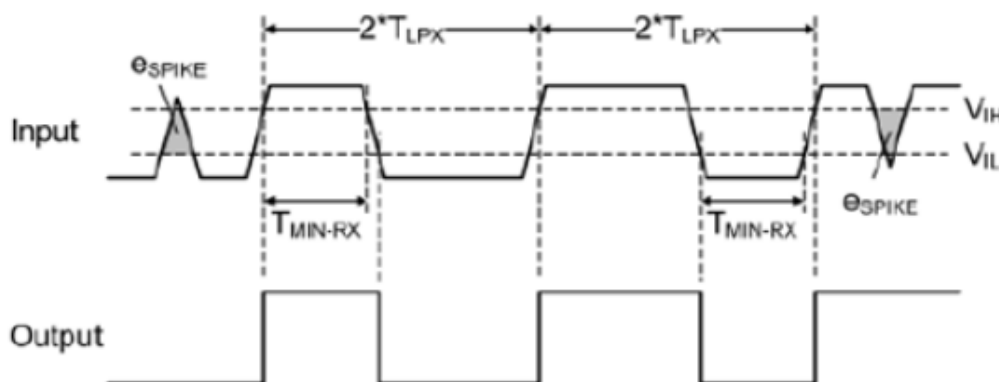
8.2.3 Line Contention Detection

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV
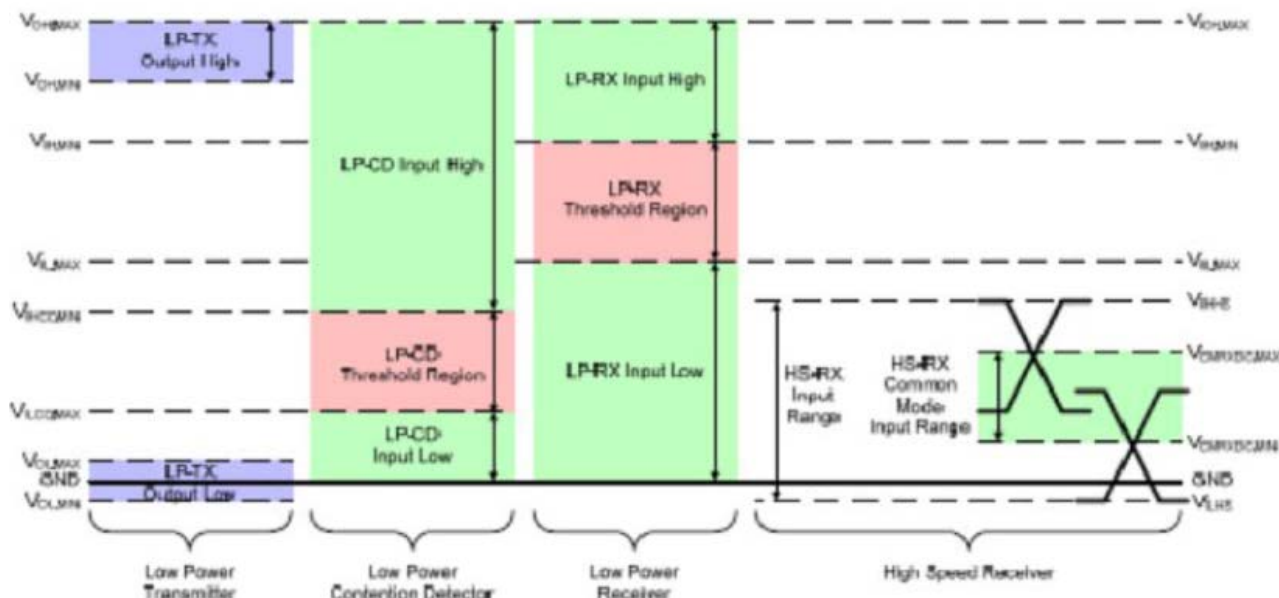
8.2.4 Input Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Pin signal voltage range	V_{PIN}	-50	-	1350	mV
Pin leakage current	V_{LEAK}	-10	-	10	uA
Ground shift	V_{GNDSH}	-50	-	50	mV
Transient pin voltage level	$V_{PIN(absmax)}$	-0.15	-	1.45	V
Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	$TV_{PIN(absmax)}$	-	-	20	ns

Notes:

1. When the pad voltage is in the signal voltage range from VGNDSH, MIN to VOH + VGNDSH, MAX and the Lane Module is in LP receive mode.

2. The voltage overshoot and undershoot beyond the VPIN is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the VPIN range.

3. This value includes ground shift.

9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	800	1000	--		Note1 Note2
Response Time		Tr+Tf	25℃	--	30	40	ms	Note1 Note3
View Angles		ΘT	CR≧10	75	80	-	Degree	Note 4
		ΘB		75	80	-		
		ΘL		75	80	-		
		ΘR		75	80	-		
Chromaticity	White	x	Brightness is on	Typ-0.05	0.305	Typ+0.05		Note5, Note1
		y			0.315			
	Red	x			0.644			
		y			0.332			
	Green	x			0.324			
		y			0.566			
	Blue	x			0.137			
		y			0.125			
Luminance		L		-	300	-	cd/m^2	Note1 Note6
Uniformity		u		75	80	-	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx
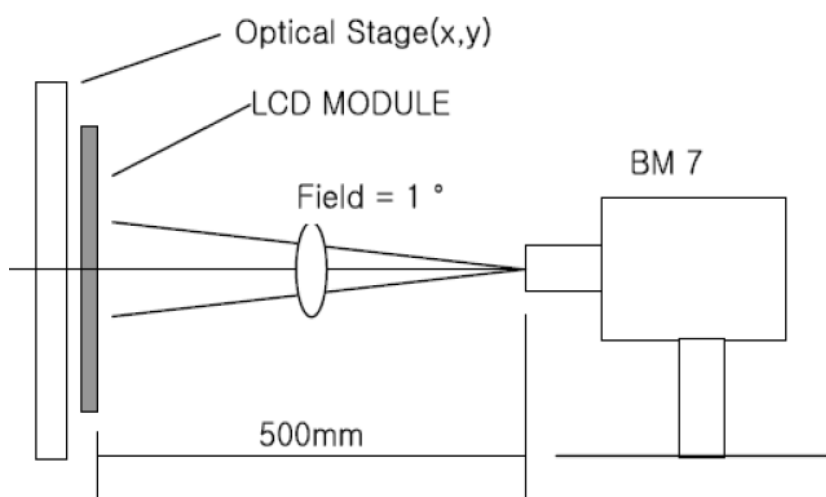
Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

Note 3: Response time is defined as follow:

   Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).
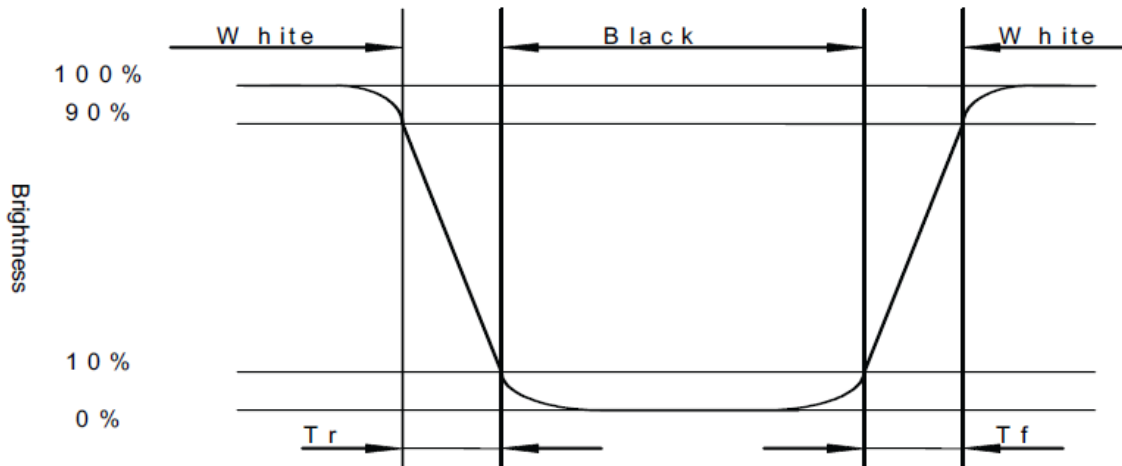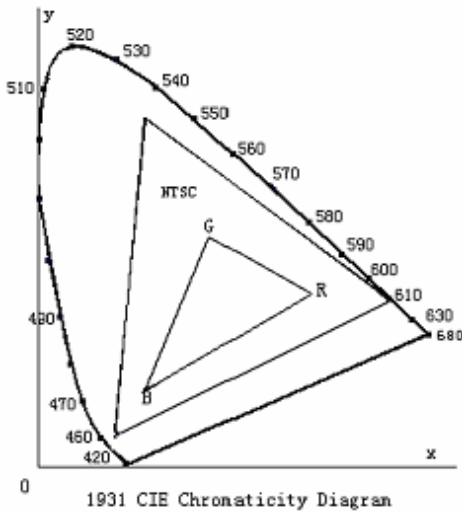

Note 4: Viewing angle range is defined as follow:

   Viewing angle is measured at the center point of the LCD.
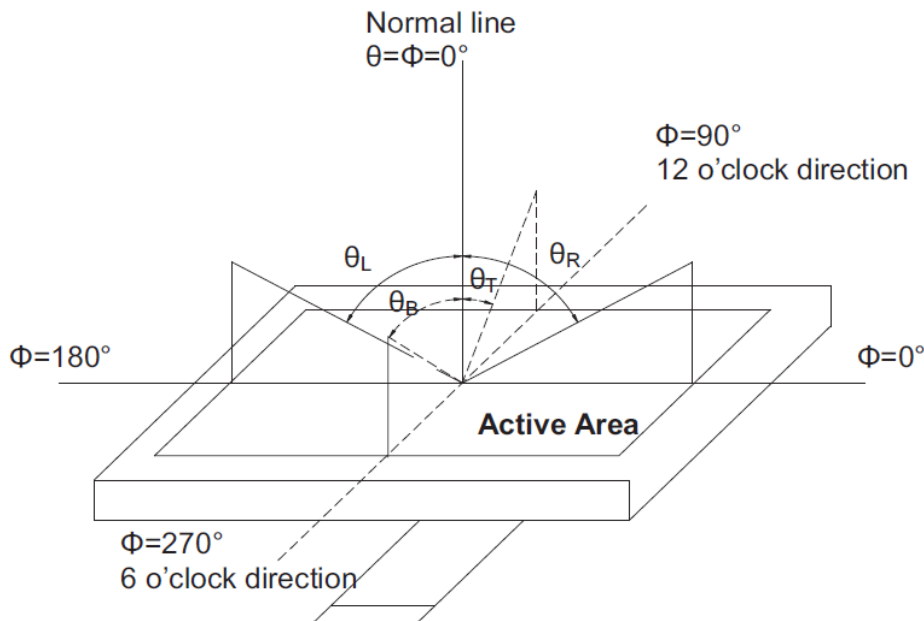
Note 5: Color chromaticity is defined as follow: (CIE1931)

   Color coordinates measured at center point of LCD.

$$S = \frac{area \ of \ RGB \ triangle}{area \ of \ NTSC \ triangle} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$
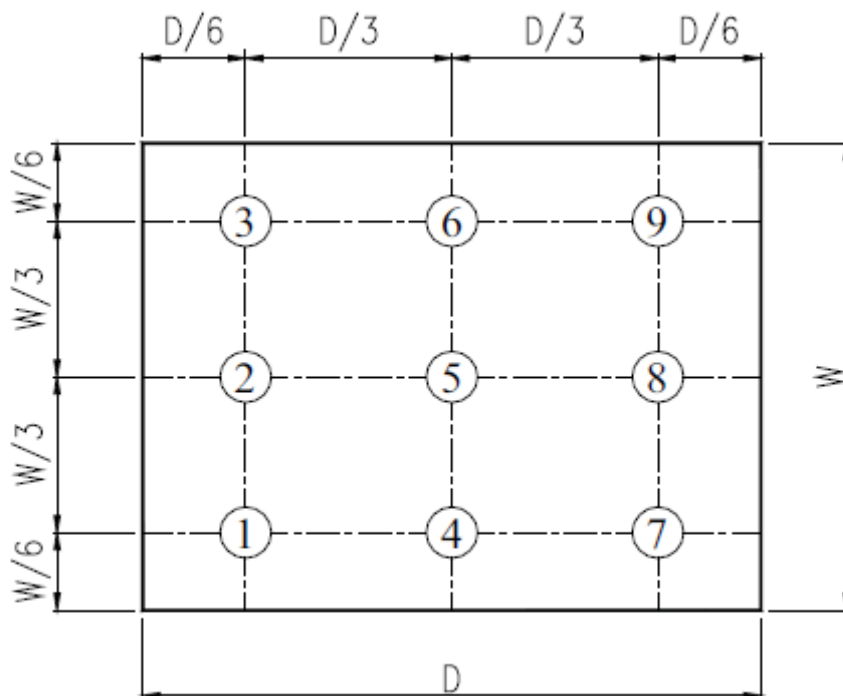
Fig. 2 Definition of uniformity

ALL SHORE INDUSTRIES

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta= +70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta= -20℃, 120hrs	Per table in below
3	High Temp Storage	Ta= +80℃, 120hrs	Per table in below
4	Low Temp Storage	Ta= -30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta= +60℃, 90% RH, 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+85℃ 30 min, Change time:5min, 5Cycles	Per table in below
7	ESD (Operation)	Air discharge:+/-8KV, Contact discharge:4KV	Per table in below
8	Vibration (Non-operation)	10Hz~150Hz, 100m/s2, 120min	Per table in below
9	Shock (Non-operation)	Half- sine wave,300m/s2,11ms	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.

B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability

C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.

D. Provide a space so that the panel does not come into contact with other components.

E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.

F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.

G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.

H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.

B. Ground your body when handling the products.

C. Power on the LCD module before applying the voltage to the input terminals.

D. Do not apply voltage which exceeds the absolute maximum rating.

E. Store the products in an anti-electrostatic bag or container.

11.4 Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.

B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.

B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

B. In order to make the display assembly stable and firm, ASI recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.

C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.