ALL SHORE INDUSTRIES

ASI-T-6951A3M4/D

Item	Contents	Unit
Size	6.95	inch
Resolution	800(RGB) x 1280	/
Interface	MIPI	/
Technology type	IPS	/
Pixel Configuration	RGB stripes	
Outline Dimension (W x H x D)	115.90x 180.80 x 4.35	mm
Active Area	94.20 x 150.72	mm
Display Mode	Normally Black	/
CTP Driver IC	GT928 or EQU	
Backlight Type	LED	/
Weight	TBD	g

Record of Revision

Date	Revision No.	Summary
2015-11-20	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of ASI-T-6951A3M4/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC,capacitive touch panel and a backlight unit. The 6.95” display area contains 800RGB) x 1280 pixels.

2. Application

Digital equipments which need color display, mobile phone,mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	6.95	inch
Resolution	800(RGB) x 1280	/
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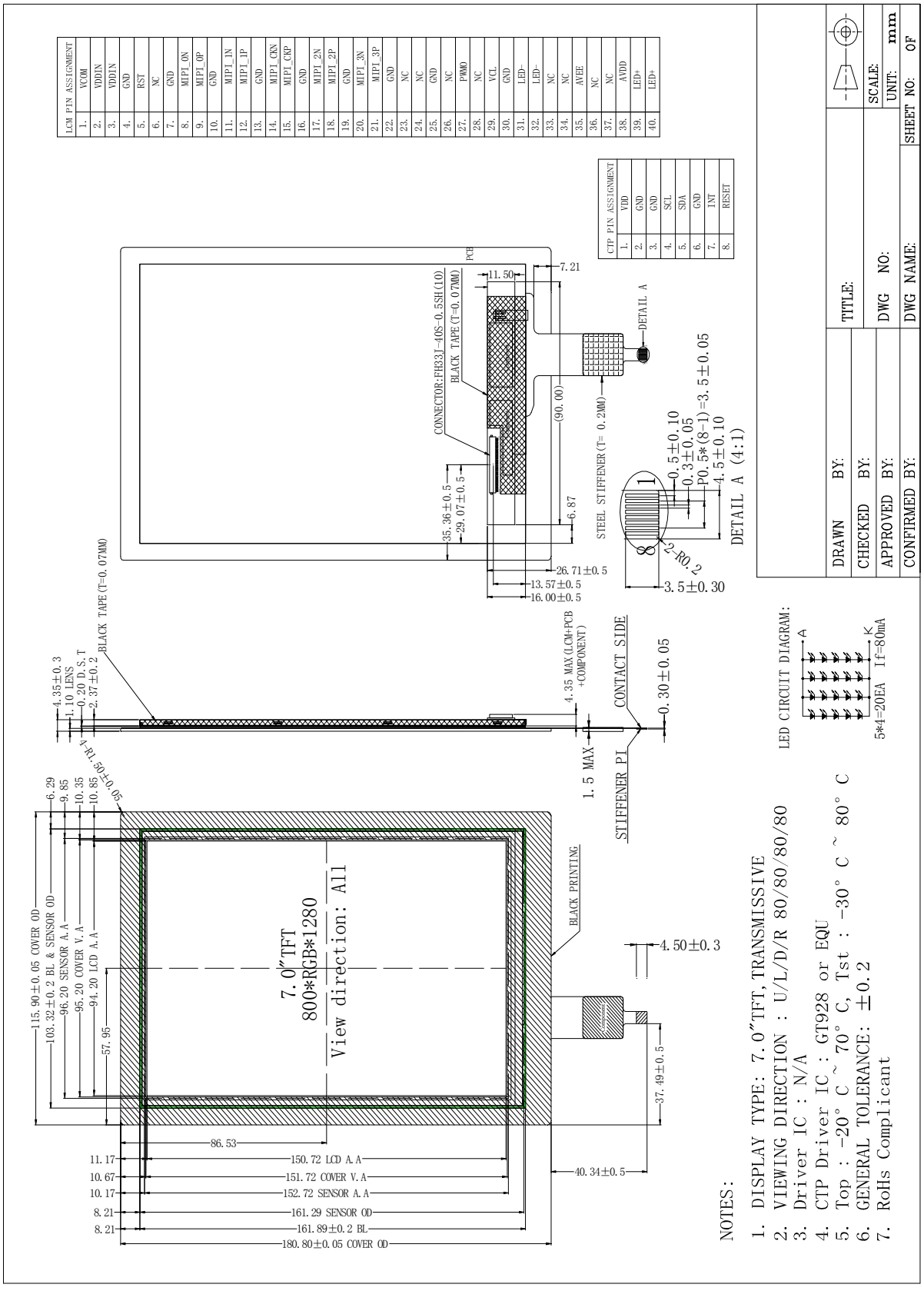
Backlight Type	LED	/
Weight	TBD	g

4. Outline Drawing



5. Interface signals

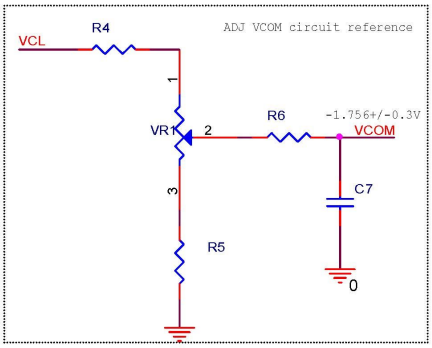
NO.	SYMBOL	DISCRIPTION	REMARK
1	VCOM	Common Voltage(-1.756 ± 0.3 V)	
2	VDDIN	Power supply for interface system except MIPI interface pin,VDDIN=3.3V	
3	VDDIN		
4	GND	GROUND	
5	RST	Device reset signal	
6	NC	No connection	
7	GND	GROUND	
8	MIPI_0N	MIPI Negative data signal (-)	
9	MIPI_0P	MIPI Positive data signal (+)	
10	GND	GROUND	
11	MIPI_1N	MIPI Negative data signal (-)	
12	MIPI_1P	MIPI Positive data signal (+)	
13	GND	GROUND	
14	MIPI_CKN	MIPI Negative clock signal (-)	
15	MIPI_CKP	MIPI Positive clock signal (+)	
16	GND	GROUND	
17	MIPI_2N	MIPI Negative data signal (-)	
18	MIPI_2P	MIPI Positive data signal (+)	
19	GND	GROUND	
20	MIPI_3N	MIPI Negative data signal (-)	
21	MIPI_3P	MIPI Positive data signal (+)	
22	GND	GROUND	
23	NC	No connection	
24	NC	No connection	
25	GND	GROUND	
26	NC	No connection	
27	PWMO	PWM control signal for LED driver (CABC)	
28	NC	No connection	
29	VCL	Output voltage pin,use it to generate Vcom voltage by a VR circuit (output voltage -2.5V)	
30	GND	GROUND	

31	LED-	LED Cathode	
32	LED-		
33	NC	No connection	
34	NC	No connection	
35	AVEE	Analog supply negative voltage	
36	NC	No connection	
37	NC	No connection	
38	AVDD	Analog supply positive voltage	
39	LED+	LED Anode	
40	LED+		

CONNECTOR:FH33J-40S-0.5SH(10)

Note

(1) Typical VCOM is only a reference value,it must be optimized according to each LCM,Be sure to use VR



(2) Global reset pin.Active Low to enter Reset State.Normally pull high.suggest to connecting with an RC reset circuit for stability.

CTP:

PIN	Symbol	Description	Remark
1	VDD	Power supply	
2	GND	Power ground.	
3	GND	Power ground.	
4	SCL	I2C data signal	
5	SDA	I2C clock signal.	
6	GND	Power ground.	
7	INT	Interrupt output Pin	
8	RESET	Reset pin	

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	Min.	TYP.	Max.	Unit	Remark
LCD Power supply	VDDIN	-0.3	-	5.5	V	
	AVDD	-0.3	-	6.6	V	
	AVEE	+0.3	-	-6.6	V	

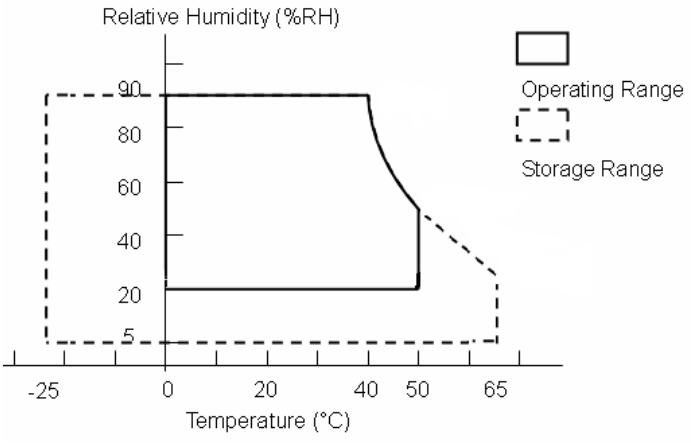
The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

Notes:

1. The relative temperature and humidity range are as below sketch, 90%RH Max. (Ta≦40℃)
2. The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing. The phenomenon is reversible.
3. If product in environment which over the definition of the relative temperature and humidity out of range too long, it will affect visual of LCD.
4. If you operate LCD in normal temperature range, the center surface of panel should be under 50℃.



7. Electrical Specifications

7.1 Electrical characteristics

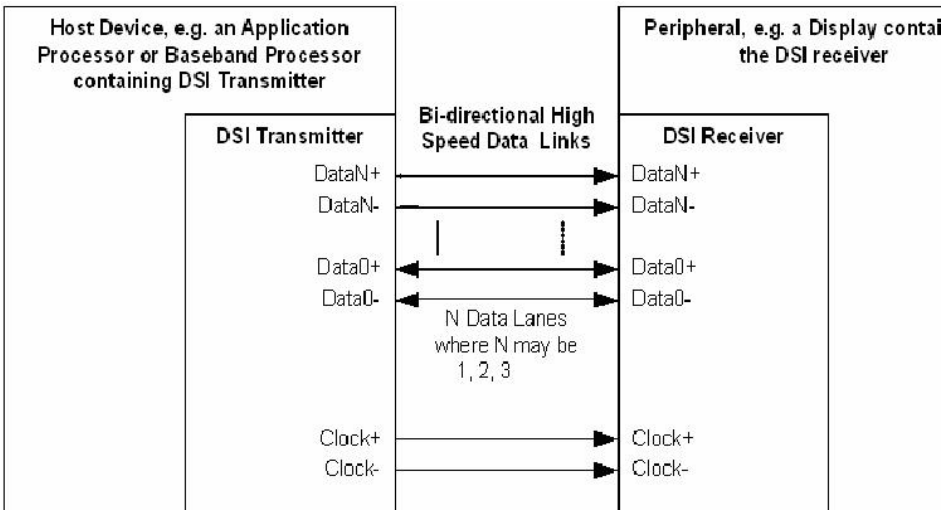
GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Input logic high voltage	VIH	0.7VDDIN	--	VDDIN	V	
Input logic low voltage	VIL	0	--	0.3VDDIN	V	
Power voltage	VDDIN	3.0	3.3	3.6	V	
	AVDD	5.2	5.8	6.0	V	
	AVEE	-6.0	-5.8	-5.2	V	
Current for Driver	IVDDIN	--	35	--	mA	
	IAVDD	--	3530	--	mA	
	IAVEE	--		--	mA	

7.2 LED Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
LED Forward Current	IF	--	80	--	mA	
LED Forward Voltage	VF	--	16	-	V	IF=80mA
LED lifetime	--	25,000	--	--	Hr	IF=80mA

7.3 Schematic of LCD module system



8. Command/AC Timing

8.1 AC Electrical Characteristics

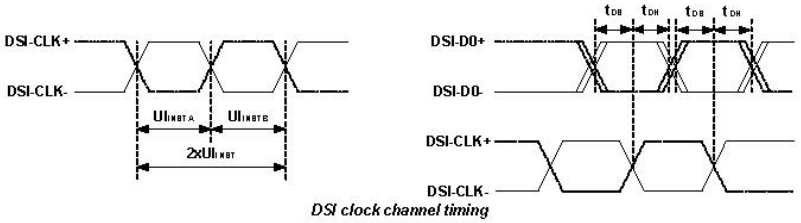
8.1.1 High Speed Mode

Signal	Symbol	Parameter	Value			Unit	Description
			Min.	Typ.	Max.		
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

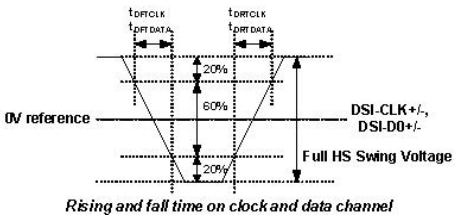
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



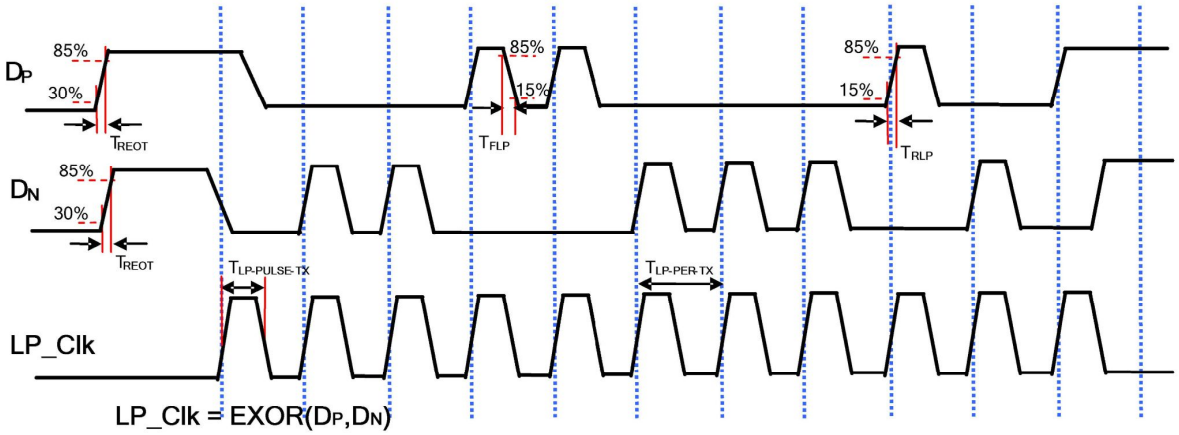
DSI clock channel timing



Rising and fall time on clock and data channel

8.1.2 LP Transmission

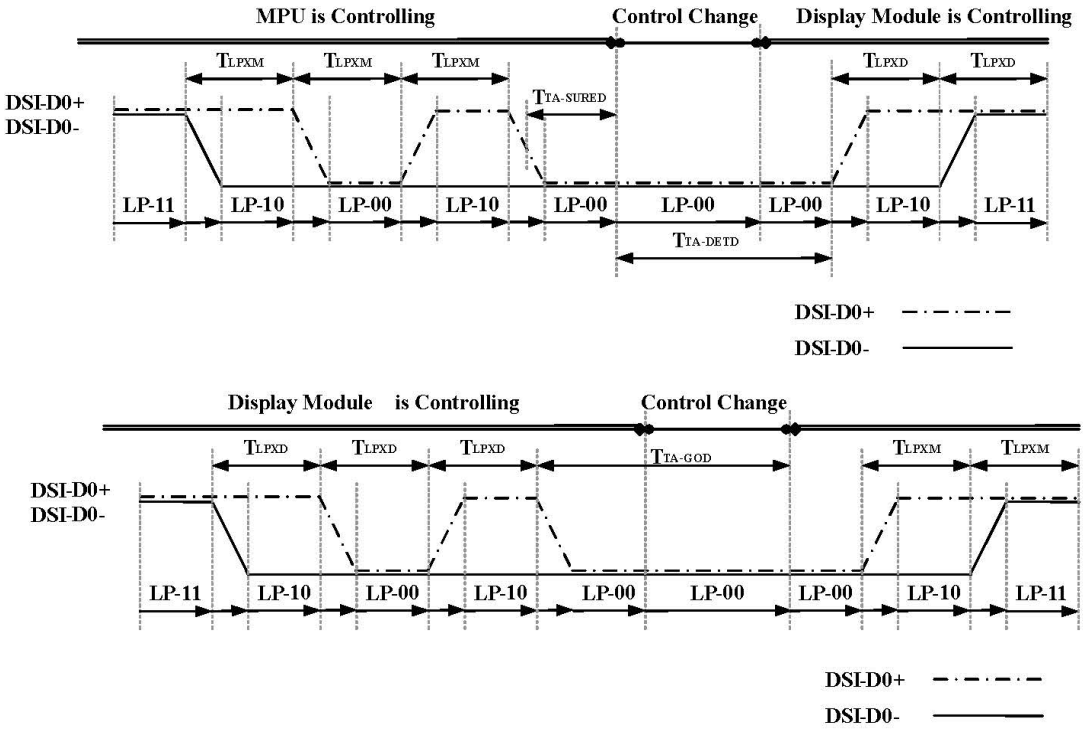
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP-PULSE-TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP-PRE-TX}$	100	130	-	ns	



8.1.3 Low Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing



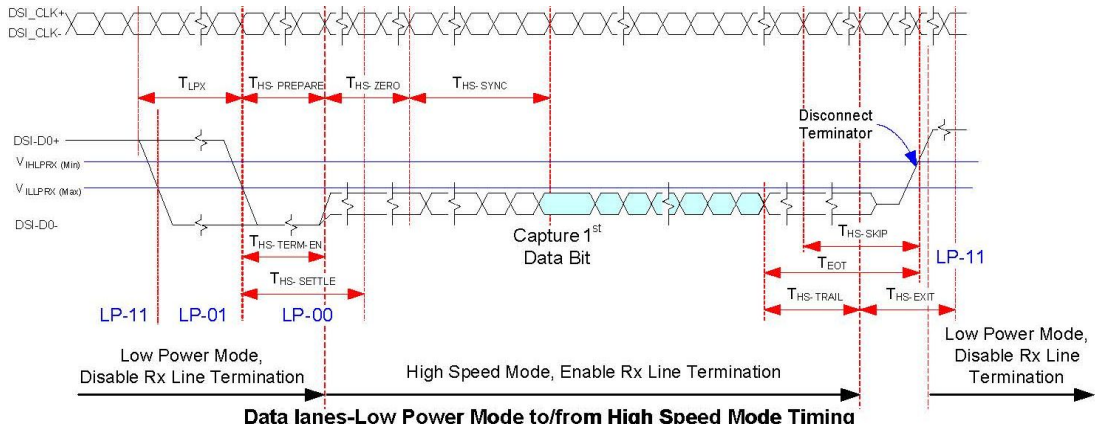
8.1.4 DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-PO	Time that the MPU shall	60+52xUI	-	-	ns	Input

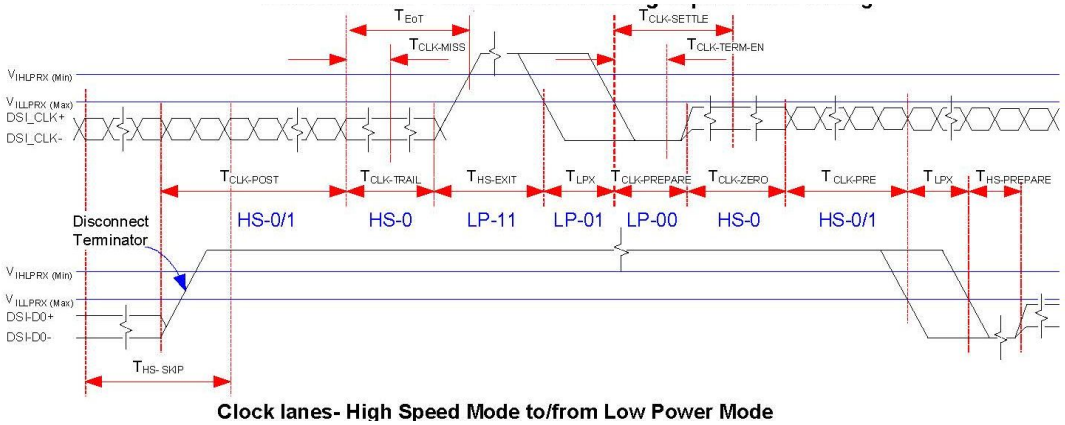
	S	continue sending HS clock after the last associated data lane has transition to LP mode					
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

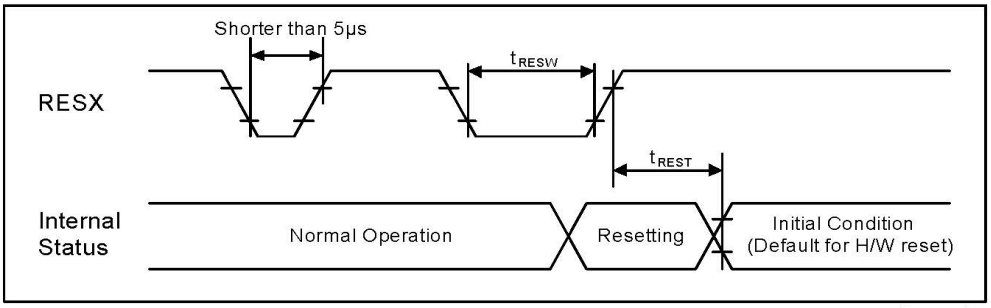


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode

8.1.5 Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

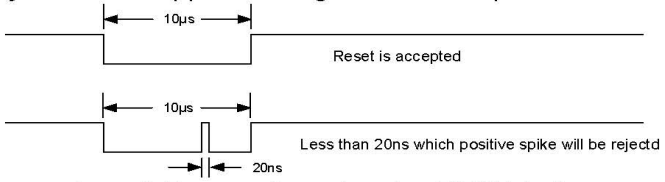
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

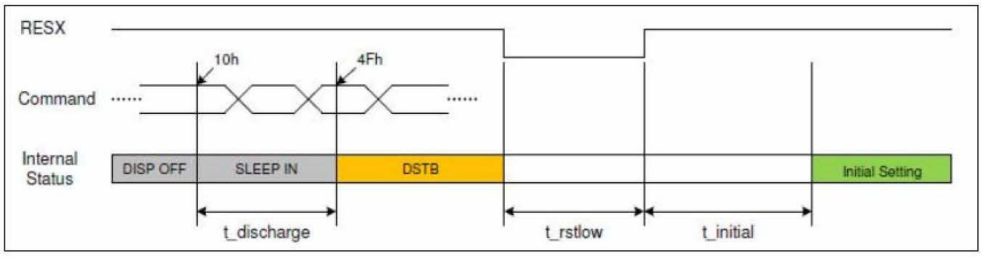
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

8.1.6 Deep Standby Mode Timing



(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,*** Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tdischarge	Sleep in into DSTB delay time	-	-	100	ms	
	trstlow	Reset low pulse	3	-	-	ms	
	tinitial	Reset high to initial setting delay time	-	-	120	ms	

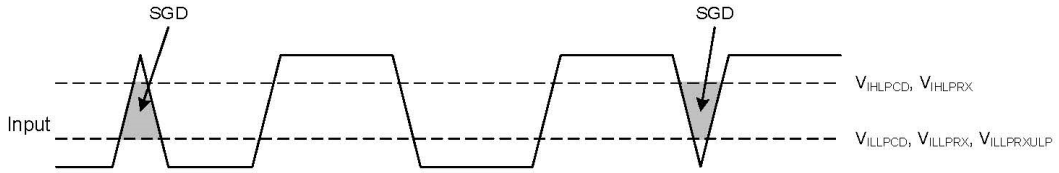
Note 1) t_discharge suggested delay time over 100ms.
Note 2) t_initial suggested delay time over 120ms..

8.2 DC Electrical Characteristics

8.2.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

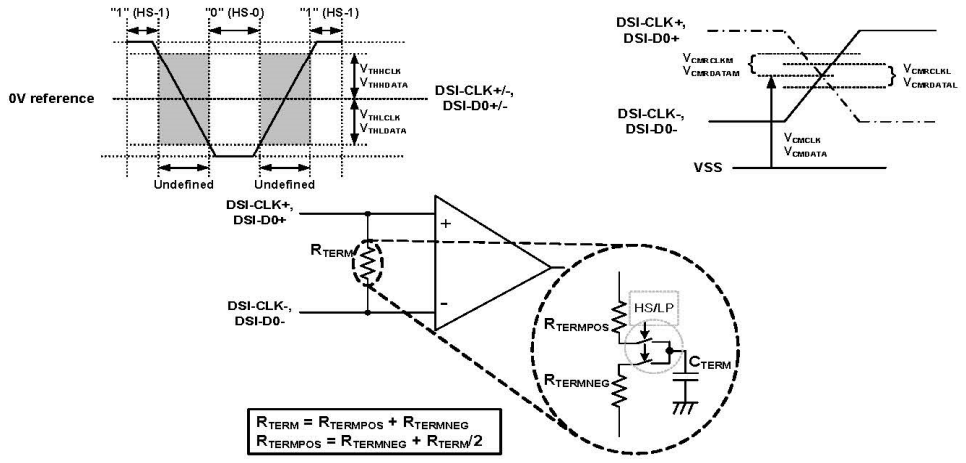


Spike/Glitch rejection-DSI

8.2.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

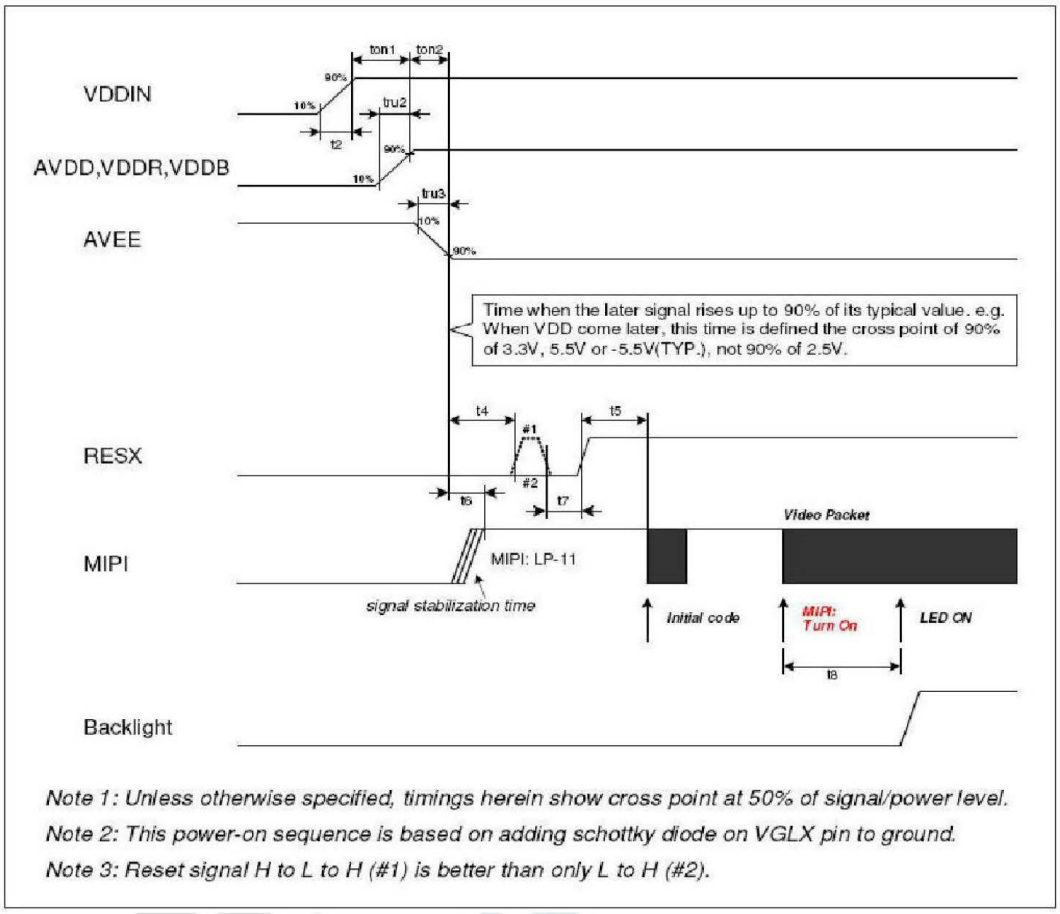
Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM.
Note 4) Without 50mV (-50mV to 50mV) ground difference.



Differential voltage range, termination resistor and Common mode voltage

8.3 POWER ON/OFF SEQUENCE

8.3.1 Power on

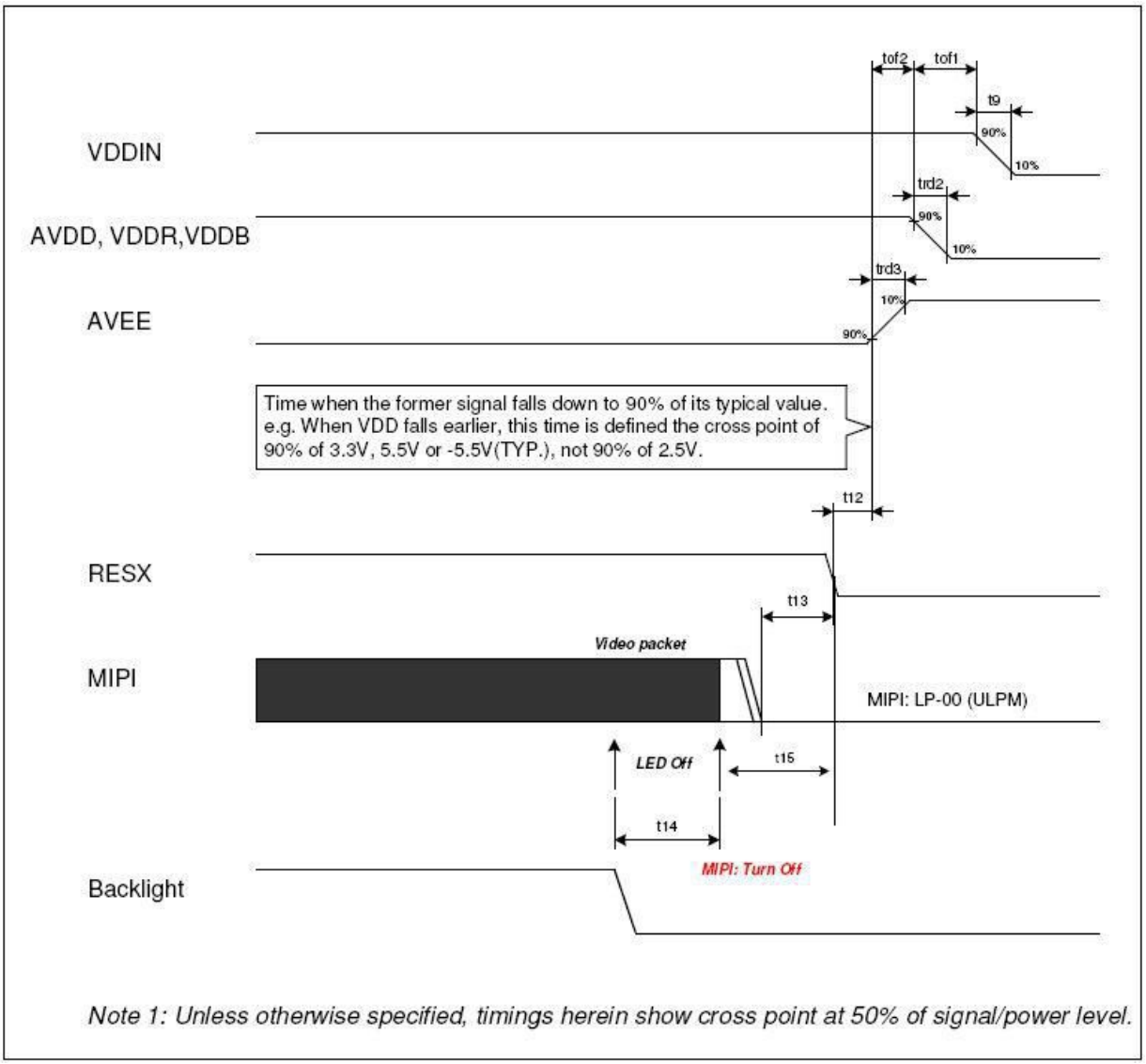


The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
ton1		No limit		ms	
ton2		0(Note)		ms	
ton3		No limit		ms	
ton4		No limit		ms	
t2	-	-	150	µs	
tru1	-	-	150	µs	
tru2	-	-	150	µs	
tru3	-	-	150	µs	
tru4	-	-	150	µs	
t4	40	-	-	ms	

t5	120	-	-	ms	
t6	0	-	-	ms	
t7	10	-	-	µs	
t8	8	-	-	Vs	Keep data more than 8 frames (VS)

8.3.2 Power off



Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1		No limit		ms	
tof2		0(Note)		ms	
tof3		No limit		ms	
tof4		No limit		μs	
trd1	150	-	-	μs	
trd2	150	-	-	μs	
trd3	150	-	-	μs	
trd4	150	-	-	μs	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	10	-	-	ms	

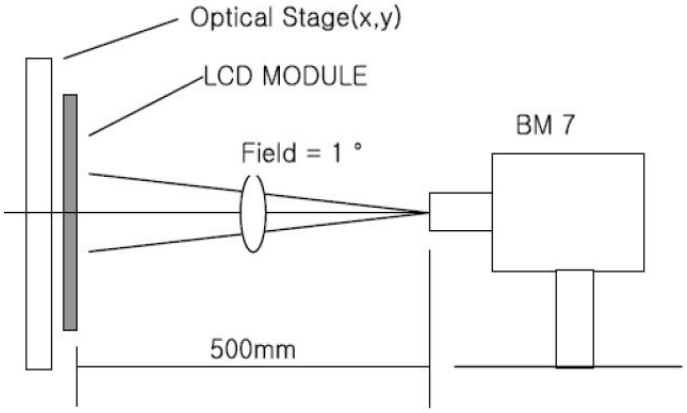
9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	600	800	-		Note1 Note2
Response Time		Tr	25℃	-	11	-	ms	Note1 Note3
		Tf		-	9	-	ms	
View Angles		θT	CR≧10	-	80	-	Degree	Note 4
		θB		-	80	-		
		θL		-	80	-		
		θR		-	80	-		
Chromaticity	White	x	Brightness is on	0.270	0.320	0.370		Note5, Note1
		y		0.280	0.330	0.380		
	Red	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
	Green	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
	Blue	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
NTSC		S		45	60	--	%	Note5
Luminance		L		250	300	--	cd/m^2	Note1 Note6
Uniformity		U		75	80	--	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃); LED back-light: ON, Environment brightness < 150 lx

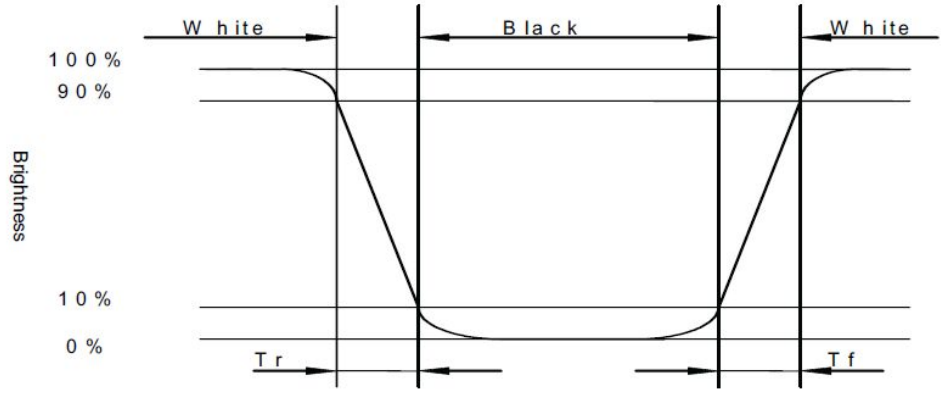


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

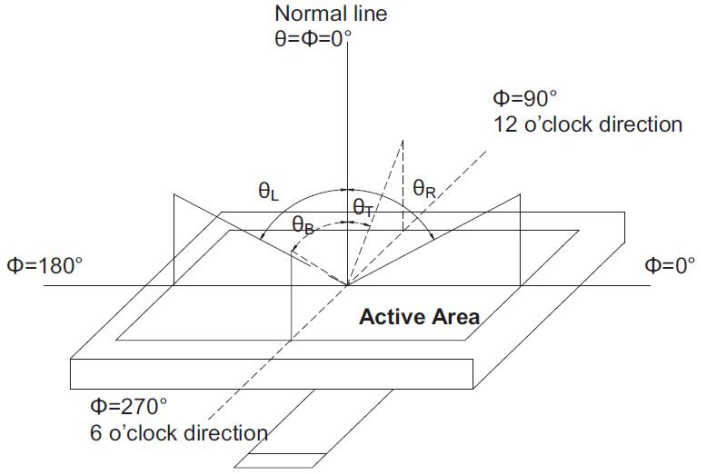
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



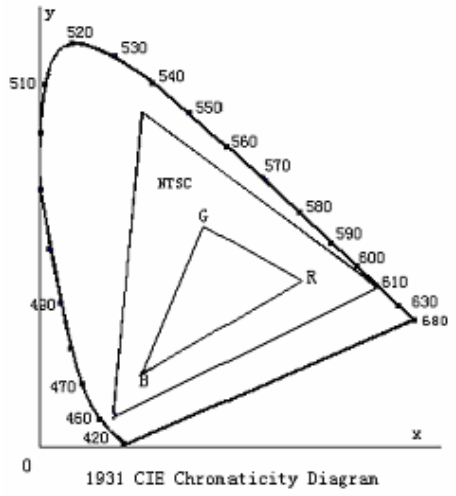
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

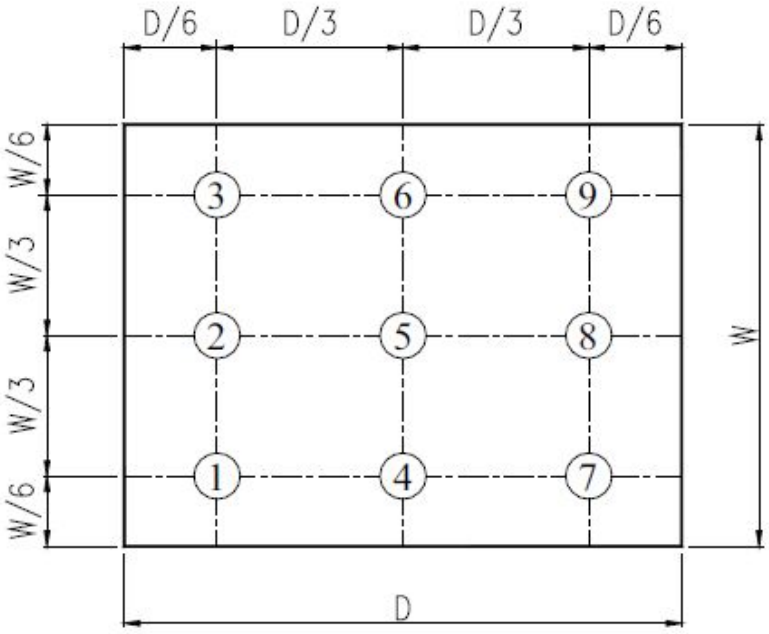


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 96hrs	Per table in below
2	Low Temp Operation	Ta=-20℃,96hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 96hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 96hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-20℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	10Hz~150Hz, 100m/s2, 120min	Per table in below
9	Shock (Non-operation)	980m/s2,Action time: 6ms, Time: 3 times for each direction, Direction:+/-X, +/-Y, +/-Z	Per table in below
10	Package Drop Test	Height:60 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

10.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.