ALL SHORE INDUSTRIES

ASI-T-5707A4MPN/D

Item	Contents	Unit
Size	5.7	inch
Resolution	720 (RGB) x 1280	/
Interface	MIPI	/
Technology type	a-Si TFT	/
Pixel pitch	0.099 x 0.099	mm
Pixel Configuration	RGB stripes	
Outline Dimension (W x H x D)	74.98 x 137.00 x 1.57	mm
Active Area	71.28 x 126.72	mm
Display Mode	Transmissive, Normally Black	/
Backlight Type	LED	/
Viewing Direction	ALL	/
Display Driver IC	OTM1287A	/
Weight	24	g

Record of Revision

Date	Revision No.	Summary
2019-02-20	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of ASI-T-5707A4MPN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver IC, FPC and a backlight unit. The 5.7″ display area contains 720(RGB) x 1280 pixels.

2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	5.7	inch
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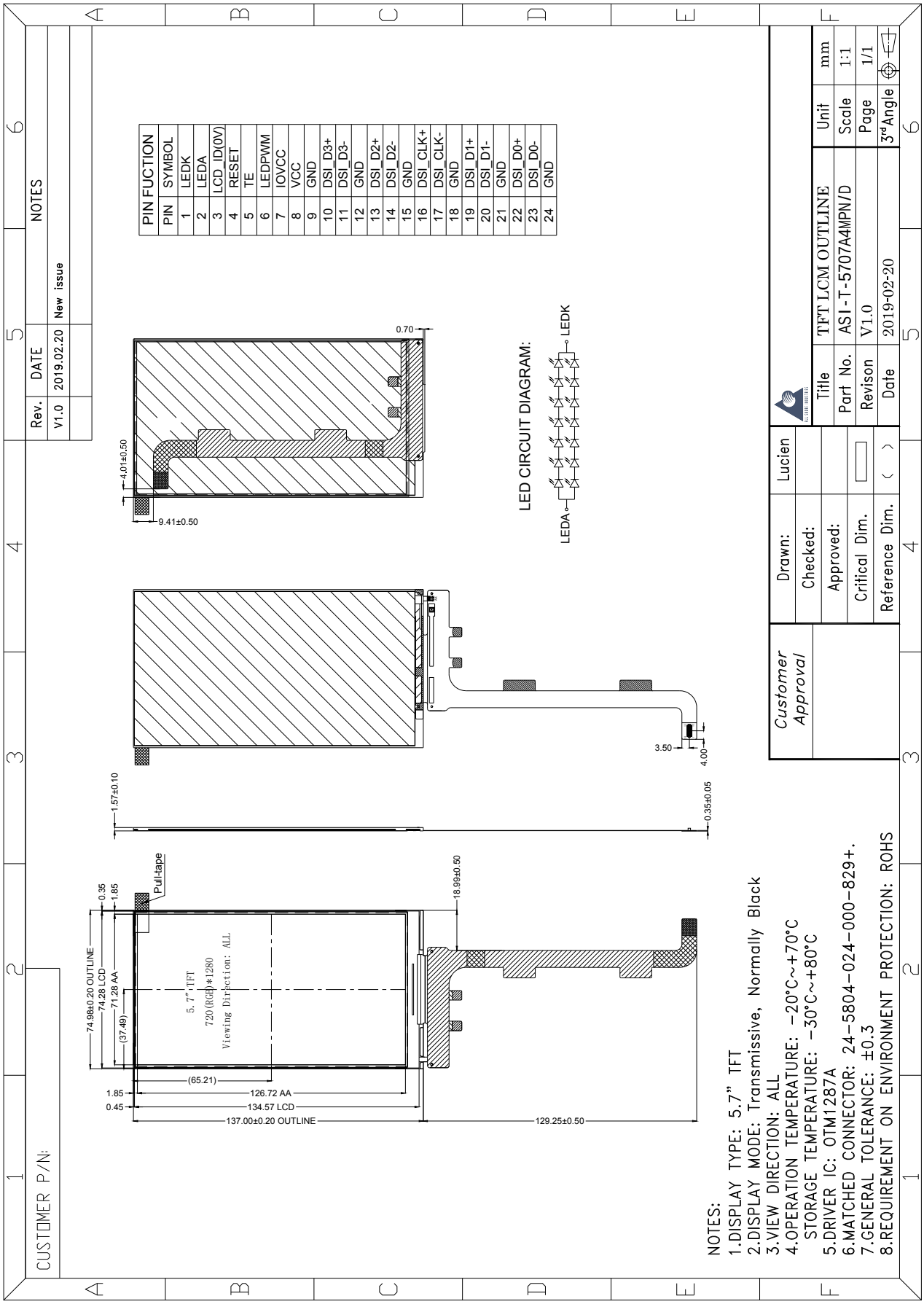
4. Outline Drawing



5. Interface signals

Pin No	Symbol	Function
1	VLEDK	Power for LED Backlight Cathode
2	VLEDA	Power for LED Backlight Anode
3	LCD_ID(0V)	LCM ID pin for customer identify (Ground)
4	RESET	Reset pin, IC is initialized when Reset is low.
5	TE	Output a frame head pulse signal
6	LEDPWM	Backlight ON/OFF control pin
7	IOVCC	Digital power supply
8	VCC	Analog supply voltage
9	GND	Power ground
10	DSI_D3+	MIPI DSI 3 lane (+)
11	DSI_D3-	MIPI DSI 3 lane (-)
12	GND	Power ground
13	DSI_D2+	MIPI DSI 2 lane (+)
14	DSI_D2-	MIPI DSI 2 lane (-)
15	GND	Power ground
16	DSI_CLK+	MIPI DSI CLK (+)
17	DSI_CLK-	MIPI DSI CLK (-)
18	GND	Power ground
19	DSI_D1+	MIPI DSI 1 lane (+)
20	DSI_D1-	MIPI DSI 1 lane (-)
21	GND	Power ground
22	DSI_D0+	MIPI DSI 0 lane (+)
23	DSI_D0-	MIPI DSI 0 lane (-)
24	GND	Power ground

Note: Matching Connection Type: 24-5804-024-000-829+.

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	IOVCC	-0.3	4.5	V	
Analog Supply Voltage	VCC	-0.3	6.0	V	
Backlight Forward Current	I_{LED}	--	25	mA	For each LED

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

Ta = 25 °C, GND=0V

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VCC	2.7	2.8	2.9	V	
		IOVCC	1.65	1.8	1.9	V	
Input voltage	“H”	VIH	0.7*IOVCC	--	IOVCC	V	
	“L”	VIL	0	--	0.3*IOVCC	V	RESET
Output voltage	“H”	VOH	0.8*IOVCC	--	IOVCC	V	
	“L”	VOL	0	--	0.2*IOVCC	V	TE, CABC
Power consumption (Panel+LSI)		White mode(60Hz)	-	320	-	mW	IOVCC=1.8V, VCC=2.8V
		Sleeping mode	-	0.05	-	mW	IOVCC=1.8V, VCC=2.8V

7.2 LED Backlight

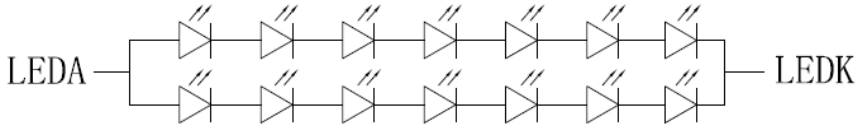
Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	40	-	mA	
Forward Voltage	VF	-	22.4	-	V	IF=40mA
LED Life time	-	-	20,000	-	Hrs	Note2

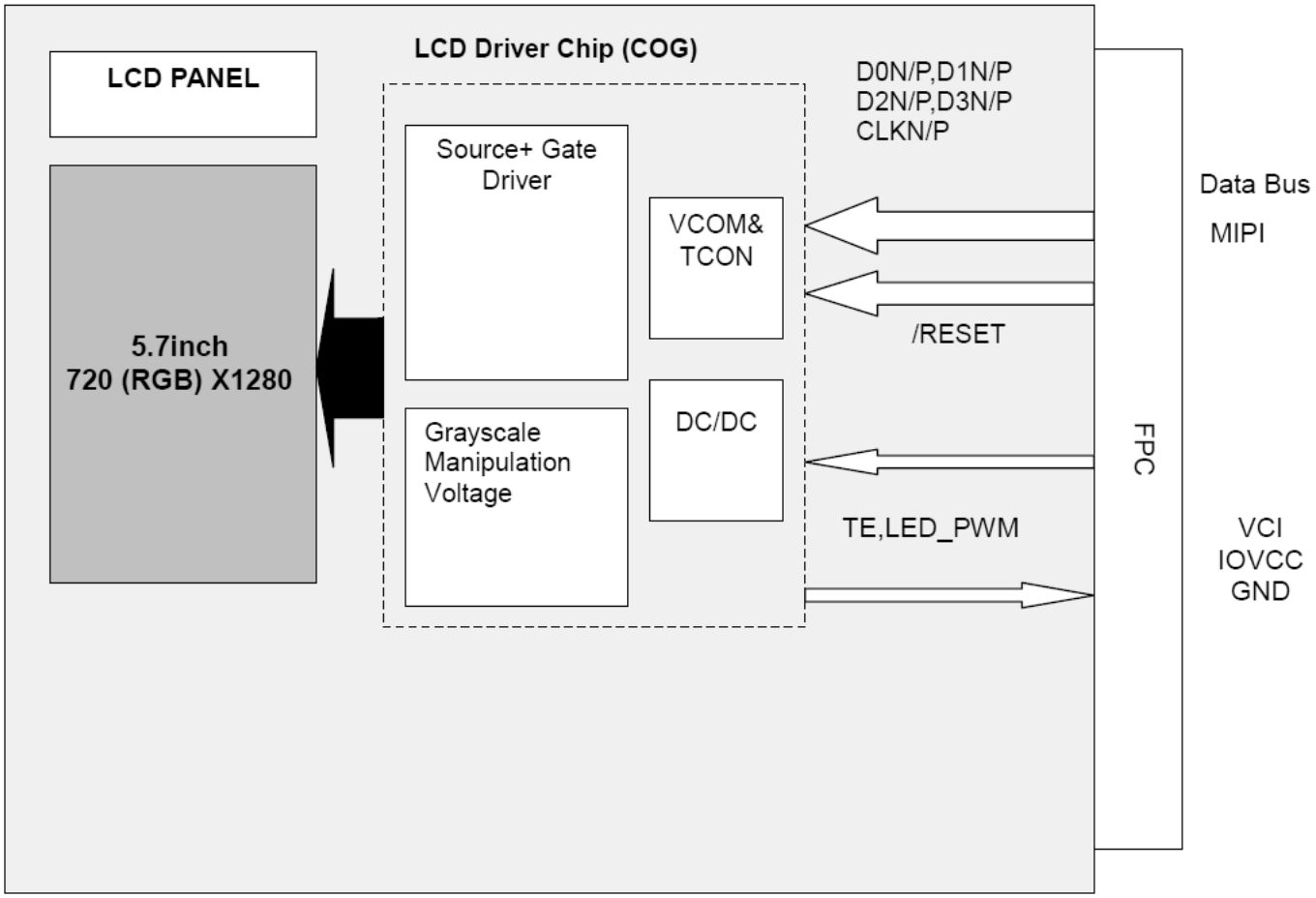
Notes:

1. One LED: IF=20mA, VF=3.2V.
2. The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IF=40mA. The LED life time could be decreased if operating IF is larger than 40mA.

LED CIRCUIT DIAGRAM:



7.3 Block Diagram



8. Command/AC Timing

8.1 The Electrical Characteristics of Low-Power Mode

Parameter	Symbol	Parameter	MIN	TYP	MAX	Unit
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP_00, LP_01, LP_10 or LP_11 periods MPU → Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP_00, LP_01, LP_10 or LP_11 periods Display Module →MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	2* T_{LPXD}	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP_00 by display module	5* T_{LPXD}	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP_00 after turnaround request - MPU	4* T_{LPXD}	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

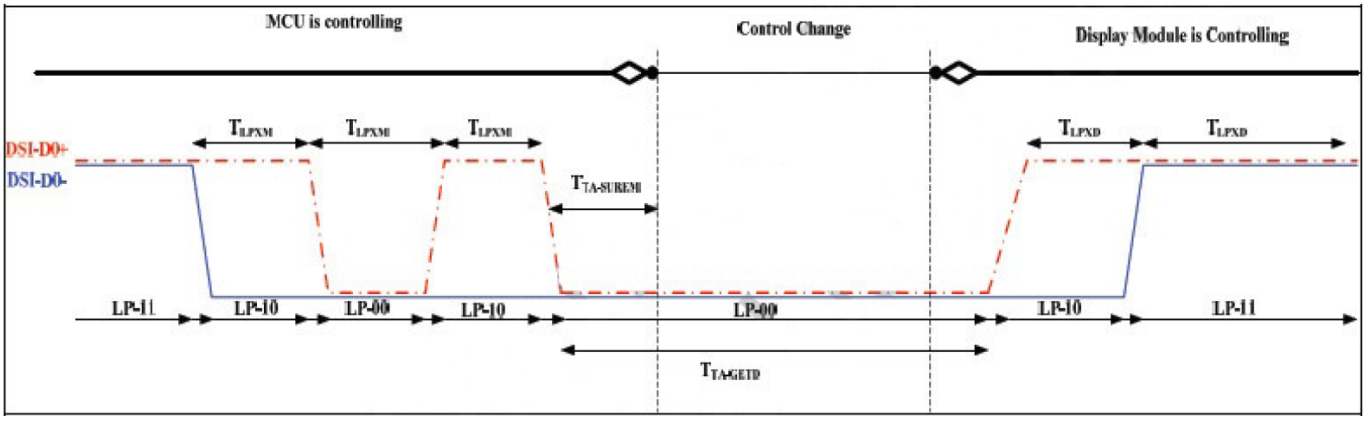


Figure: BTA from the MCU to the Display Module

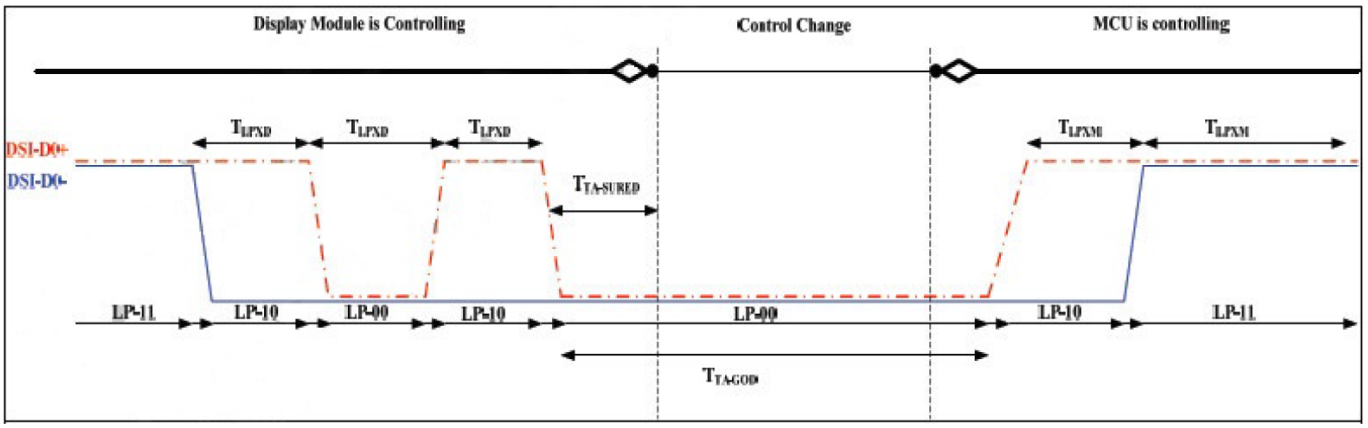
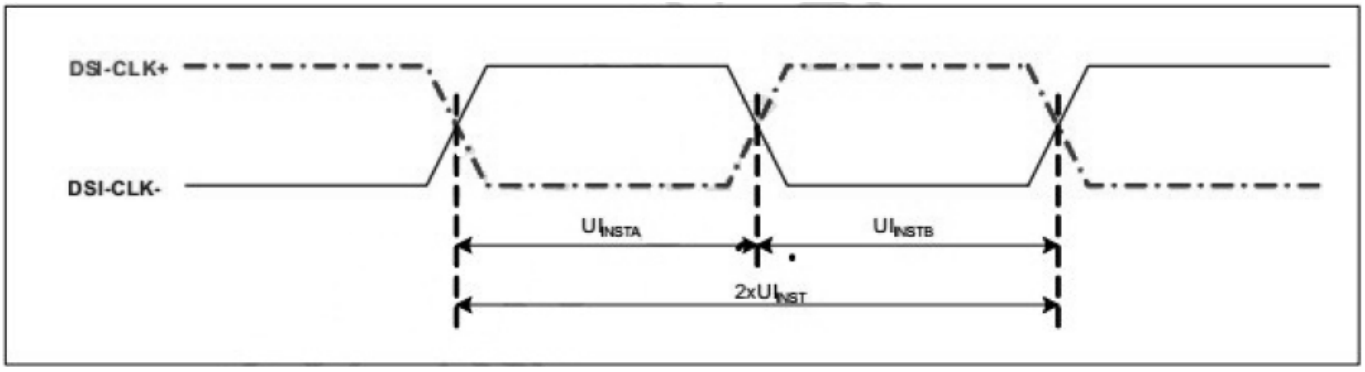


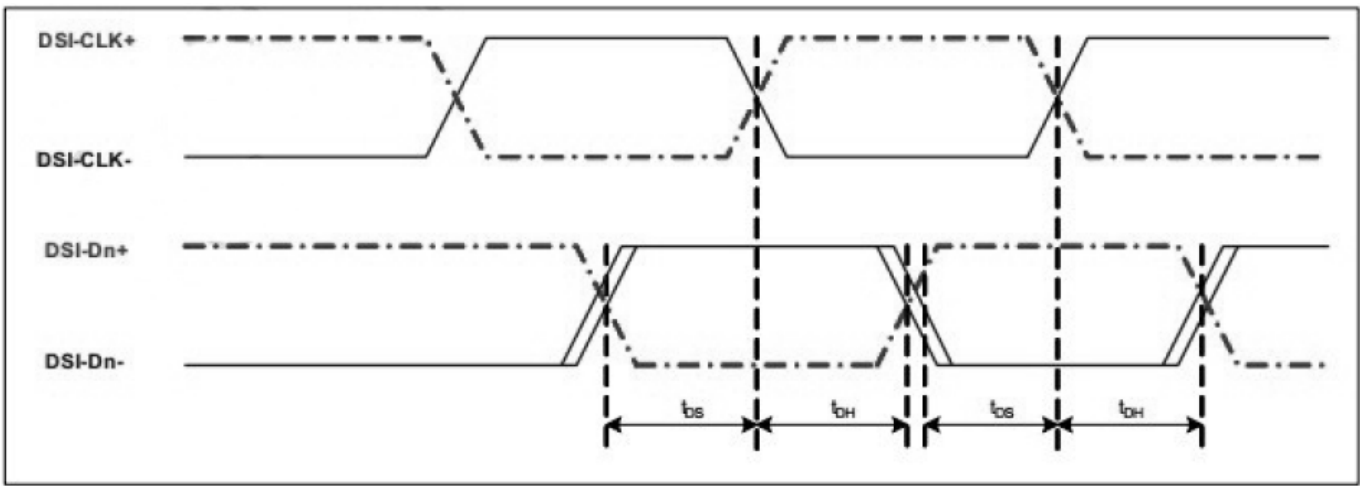
Figure: BTA from the Display Module to the MCU

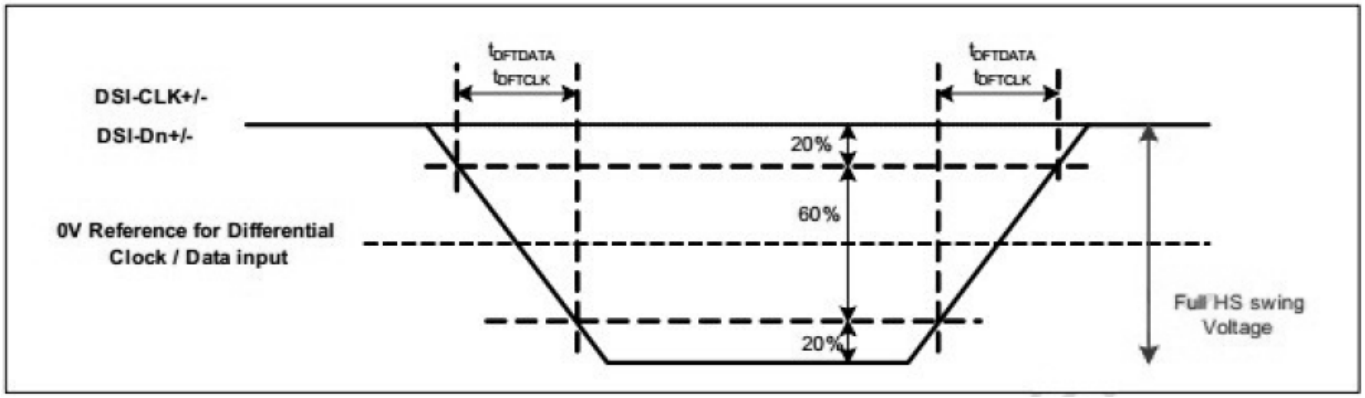
8.2 The Electrical Characteristics of High-Speed Mode

Parameter	Symbol	Parameter	MIN	TYP	MAX	Unit
High Speed Mode						
DSI-CLK+/-	2*UI_{INST}	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns

DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps







8.3 Bursts

Parameter	Symbol	Parameter	MIN	TYP	MAX	Unit
High Speed Data Transmission Bursts						

DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP_00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$, $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS_0 before the sync sequence	145ns+10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach $V_{TERM-EN}$	-	35ns+4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-0ut at RX to ignore transition period of EOT	40	-	55ns+4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	Max(8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP_11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EOT}	Time from start of $T_{HS-TRAIL}$ period to start of LP_11 state	-	-	105ns+12 UI	ns

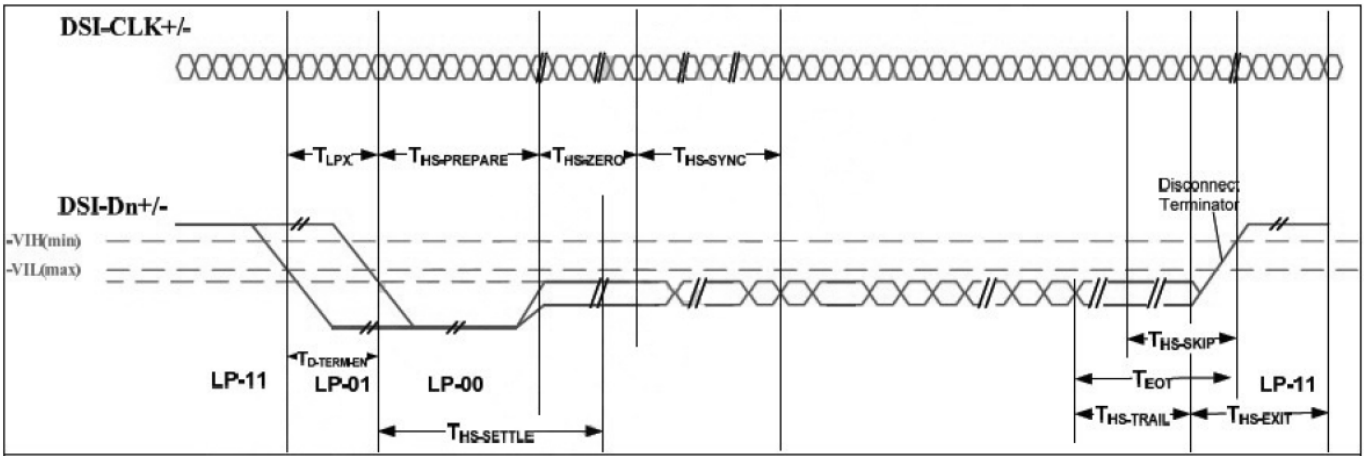


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	MIN	TYP	MAX	Unit
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{HS-PREPARE}$, $T_{HS-ZERO}$	Time to drive LP_00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EM}$	Time to enable clock Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$, $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS_0 drive period before starting clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EOT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP_11 state	-	-	105ns+12 UI	ns

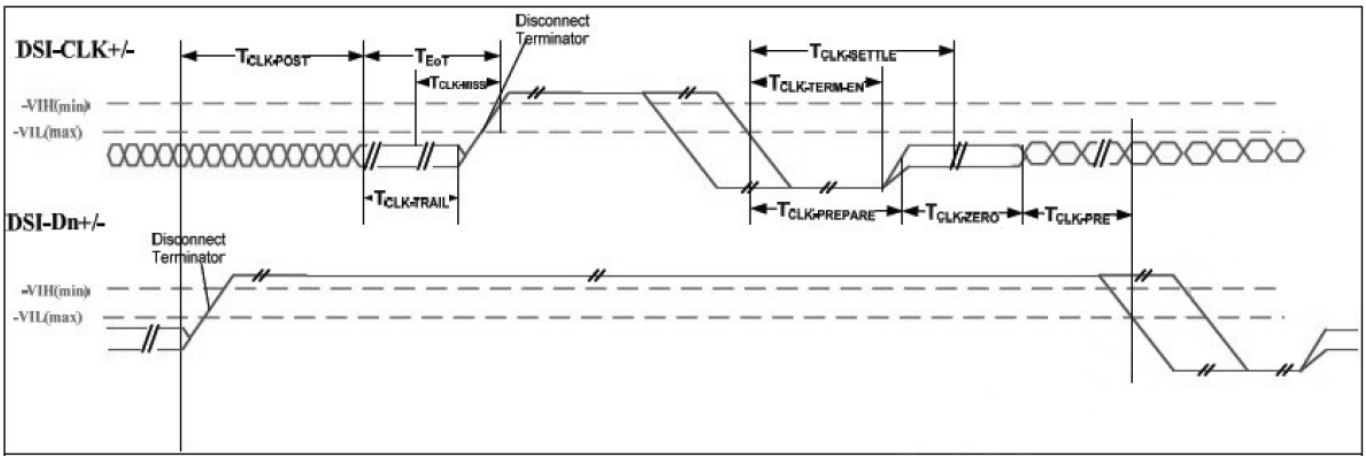


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

8.4 LP-11 Between High Speed and Low Power Mode

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

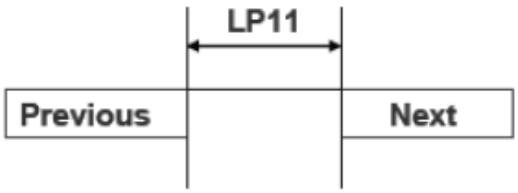
1. High Speed Mode =>Stop State(SS,LP-11)=>High Speed Mode
2. High Speed Mode =>Stop State(SS,LP-11)=>Low Power Mode
3. Low Power Mode=>Stop State(SS,LP-11)=>High Speed Mode
4. Low Power Mode=>Stop State(SS,LP-11)=>Low Power Mode

The Low Power Mode is also including 2 different functions:

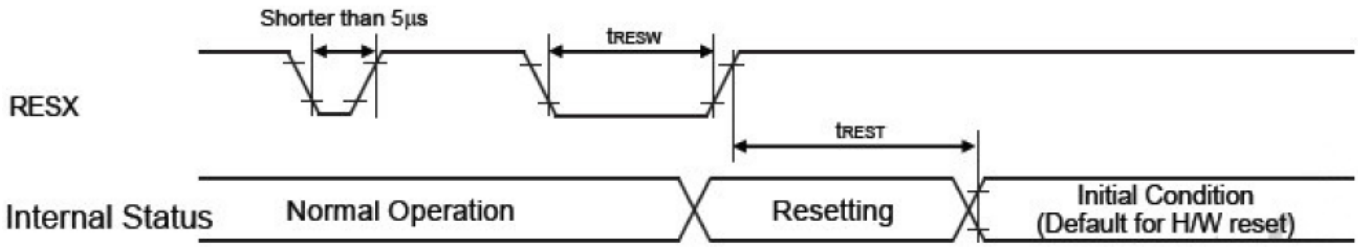
1. Escape
2. Bus Turnaround (BTA)

Stop state (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-



8.5 Reset Timing Characteristics



Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	1)Reset low pulse width	RESX	10	-	-	-	us
tREST	2)Reset complete time	-	-	-	5	When reset applied during sleep in mode	ms
		-	-	-	120	When reset applied during sleep out mode	ms

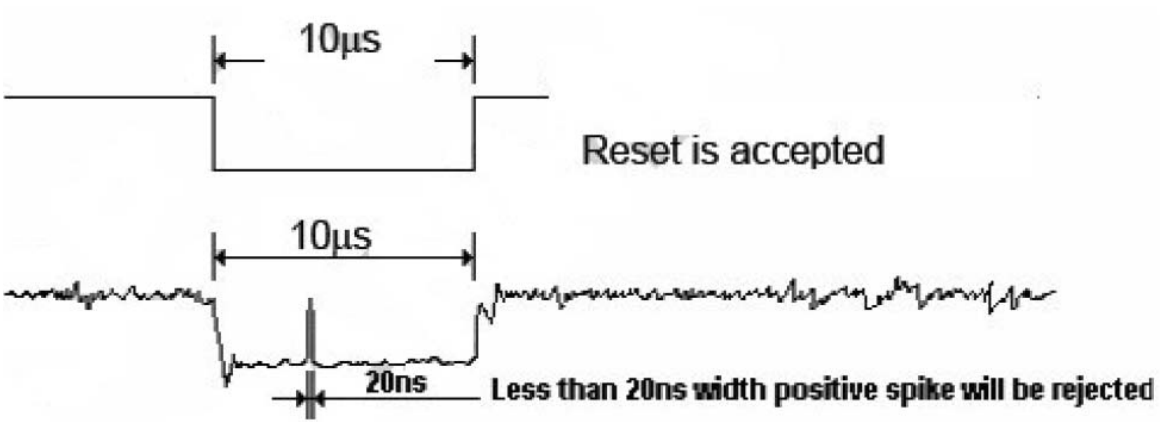
Note1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5μS	Reset Rejected
Longer than 10μS	Reset
Between 5μS and 10μS	Reset starts (It depends on voltage and temperature condition.)

Note2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

Note3: During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note4: Spike Rejection also applies during a valid reset pulse as shown below:

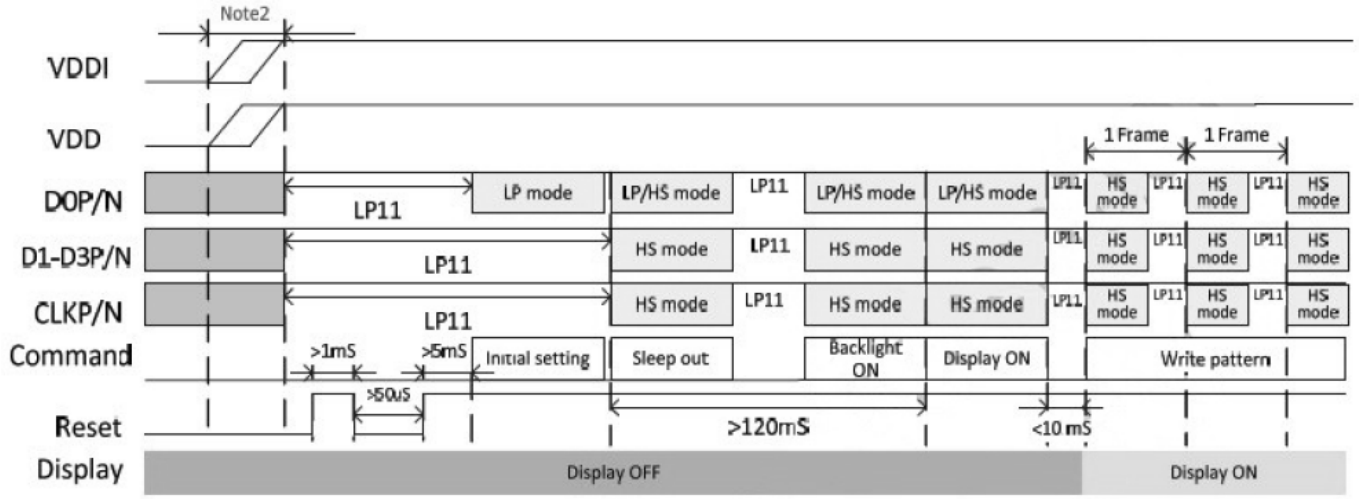


Note5: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep out command cannot be sent for 120msec.

8.6 Power ON/OFF Sequence

8.6.1 Power on Sequence with MIPI video timing

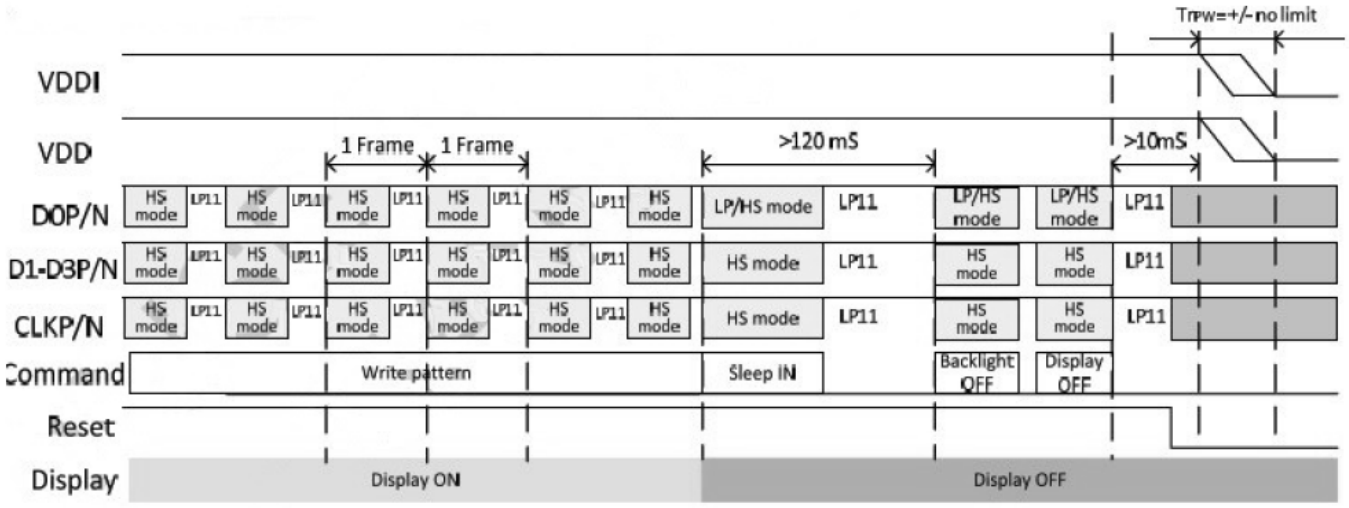
Power ON Sequence



Note1: Propose using non-continuous CLK with Burst mode.
Note2: For VDDI/VDD power, propose applying them separately and having 10ms timing gap.

8.6.2 Power off Sequence with MIPI video timing

Power OFF Sequence



Note1: Propose using non-continuous CLK with Burst mode.

Note:
1, Sleep out (Low Power mode)
2, Display on (Low Power mode)
3, Display off (Low Power mode)
4, Sleep in.

9. Optical Specification

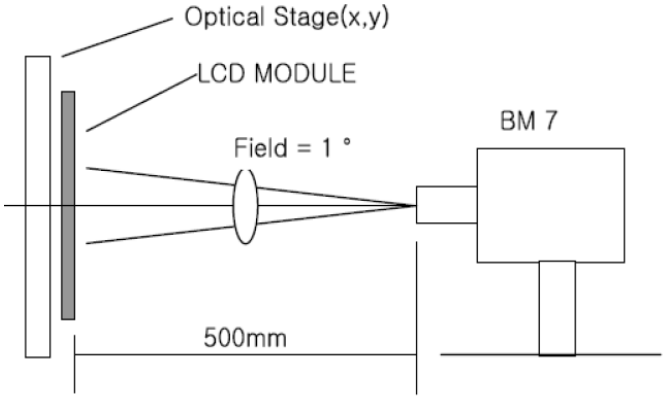
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	700	900	-		Note1 Note2
Response Time		Ton/ Toff	25℃	-	25	35	ms	Note1 Note3
View Angles		ΘT	CR≧10	80	85	-	Degree	Note 4
		ΘB		80	85	-		
		ΘL		80	85	-		
		ΘR		80	85	-		
Chromaticity	White	x	Brightness is on	0.250	0.300	0.350		Note5, Note1
		y		0.278	0.328	0.378		
	Red	x		0.584	0.634	0.684		
		y		0.290	0.340	0.390		
	Green	x		0.269	0.319	0.369		
		y		0.572	0.622	0.672		
	Blue	x		0.102	0.152	0.202		
		y		0.009	0.059	0.109		
Luminance		L		400	450	-	cd/m^2	Note1 Note6
Uniformity		U		80	85	-	%	Note1 Note7
NTSC Ratio		S		65	70	-	%	

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

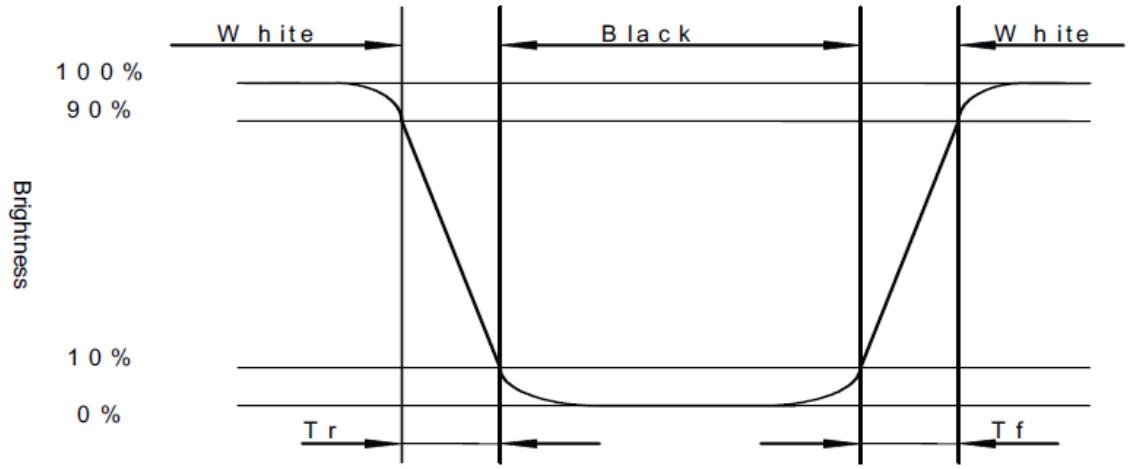


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

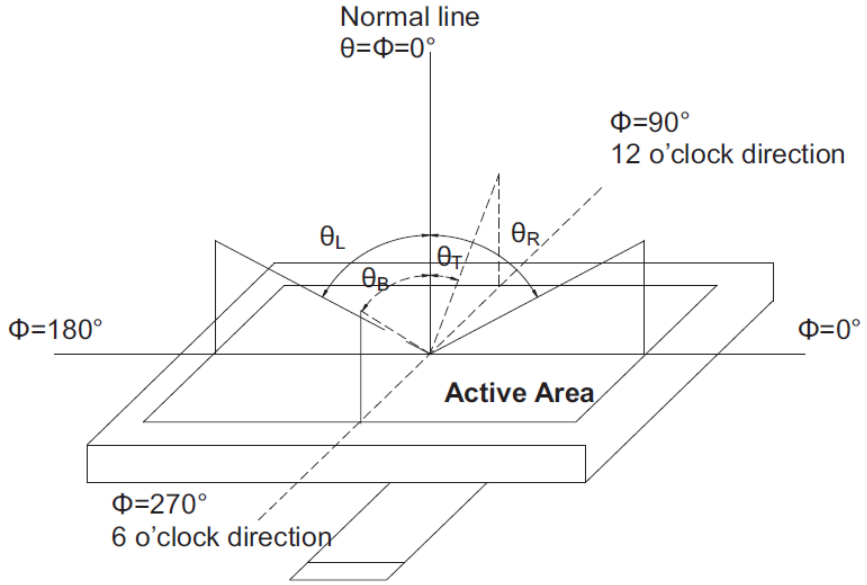
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



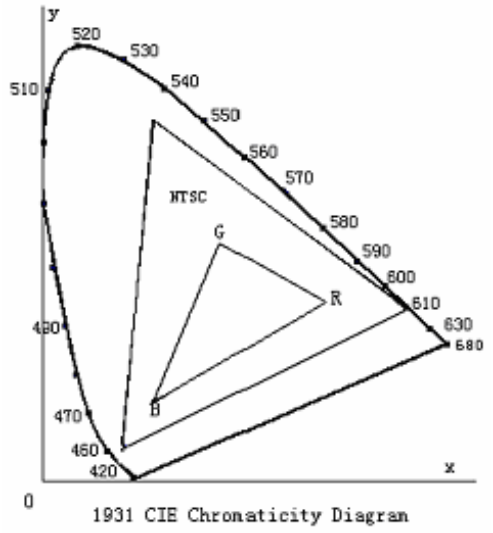
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

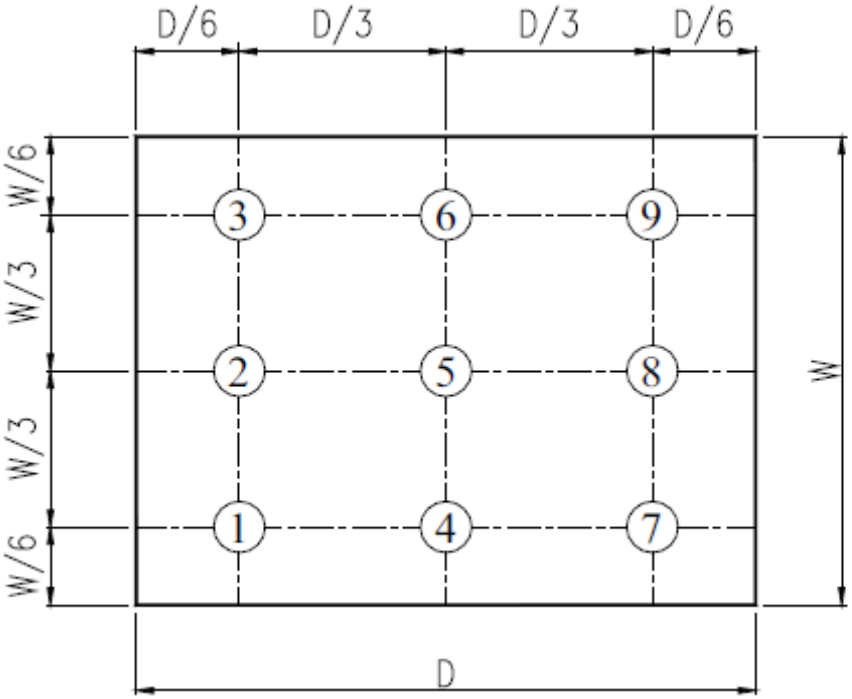


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+80℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 120hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+80℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.
F. Peel off the LCM protective film slowly since static electricity may be generated.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, ASI recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.