ALL SHORE INDUSTRIES

ASI-T-400R72A3MPN/X

Item	Dimension	Unit
Size	4.0	inch
Dot Matrix	720 x RGB x 720 (TFT)	dots
Module dimension	105.3 x 109.62 x 2.3	mm
Active area	101.52 x 101.52	mm
Pixel pitch	0.141 X 0.141	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing Angle	85/85/85/85	
TFT Interface	4-Lanes MIPI	
Backlight Type	LED ,Normally White	
TFT Driver IC	FL7703 or Equivalent	
With /Without TP	Without TP	
Surface	Anti-Glare	

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2025/01/13		First issue
A	2025/02/26		Add Black Mylar sheet

Contents

1.General Specifications

Item	Dimension	Unit
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Backlight Type	LED ,Normally White	
TFT Driver IC	FL7703 or Equivalent	
With /Without TP	Without TP	
Surface	Anti-Glare	

*Color tone slight changed by temperature and driving voltage.

2.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦ 60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

3.Electrical Characteristics

3.1. Operating conditions

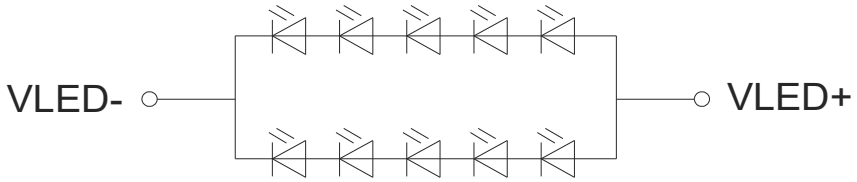
VCI=3.3V， GND=0V， Ta = 25 ℃

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital supply Voltage		IOVCC	1.65	1.8	3.3	V	
Analog supply Voltage		VCI	2.8	3.0	3.3	V	
Input Signal Voltage	Low Level	VIL	0	-	0.3 x IOVCC	V	
	High Level	VIH	0.7 x IOVCC	-	IOVCC	V	
Current of digital supply voltage		IIOVCC	-	15	20	mA	VCI=3.3V, color bar pattern
Current of analog supply voltage		IVCI	-	35	50	mA	

3.2. LED driving conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	-	-	40	45	mA	-
LED voltage	VLED+		15.5	16.0	V	Note 1
Backlight Power Consumption	WBL	-	600	720	mW	
LED Life Time	-	30,000	-	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



Backlight Circuit

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

4.MIPI DC Characteristic

4.1. DSI DC Characteristics

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

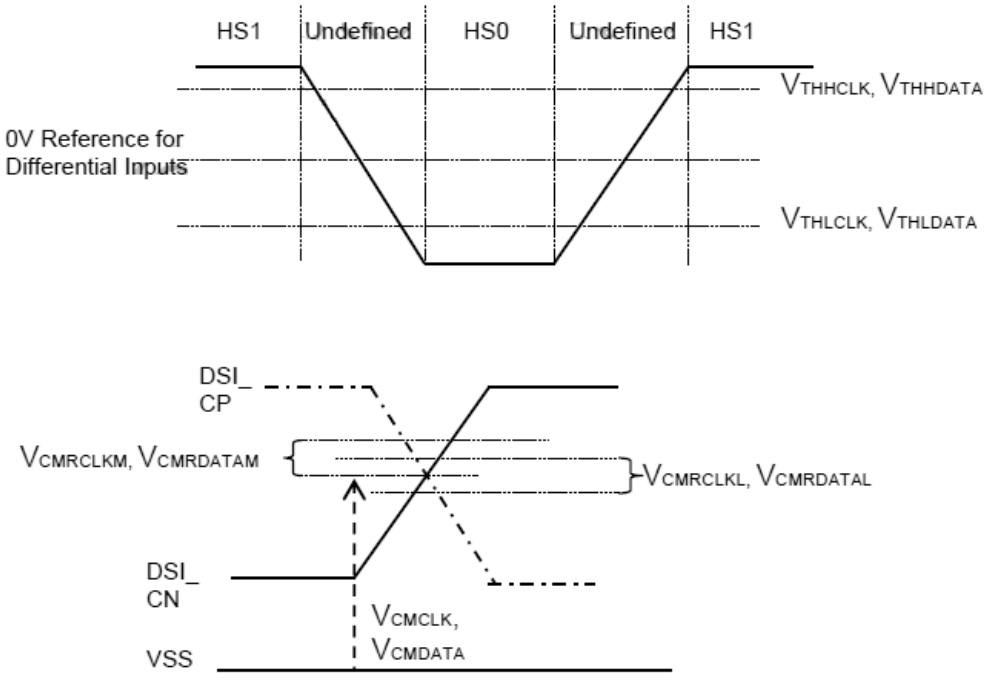


Figure 1: Differential voltage range and Command mode voltage

5.Timing Chart

5.1. DSI Interface Timing Characteristics: high speed mode-clock channel timing

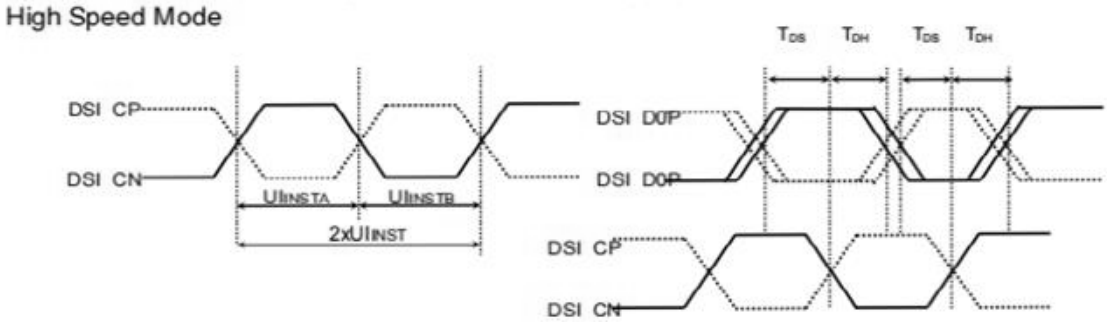
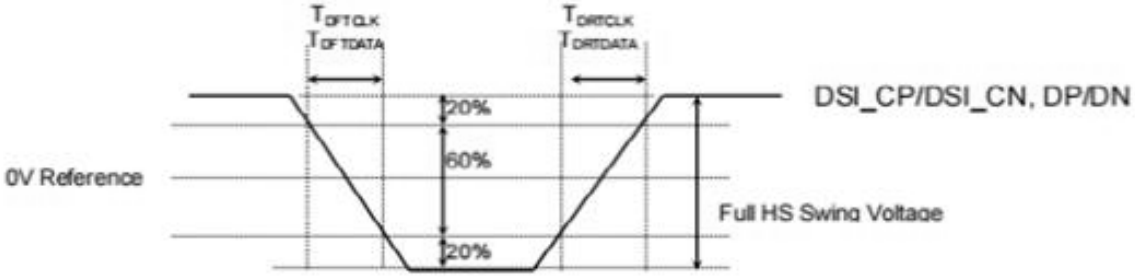


Figure 2: DSI clock timing characteristics

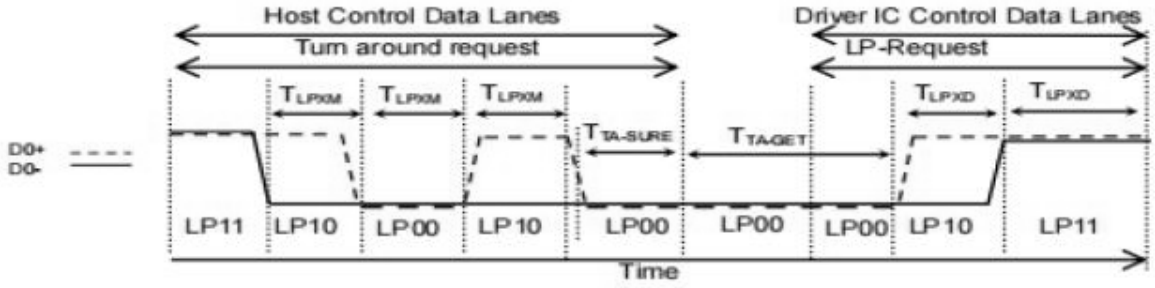


Rising and falling time on clock and data channel

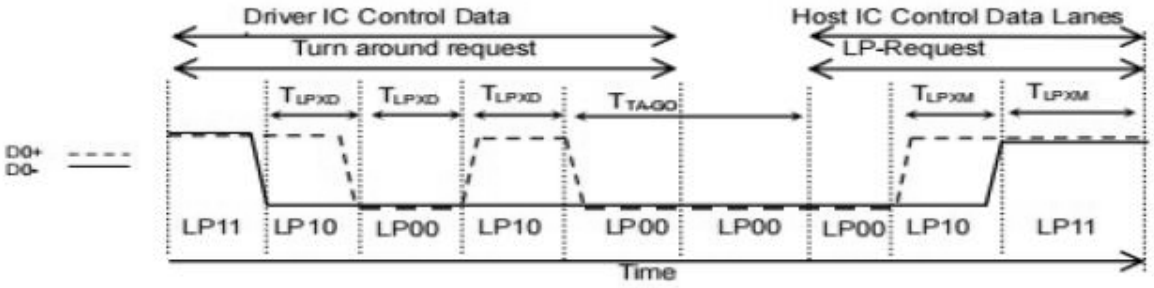
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	4LANE: 3.30 3LANE: 2.85 @ VDDD=1.8V	-	25	ns
	UI instantaneous	UINSTA UINSTB	4LANE: 1.67 3LANE: 1.43 @ VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Low Power Mode



BTA from HOST to Display Module Timing



BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

DSI Low Power Mode Characteristics

5.2. Recommended Timing Setting of TCON

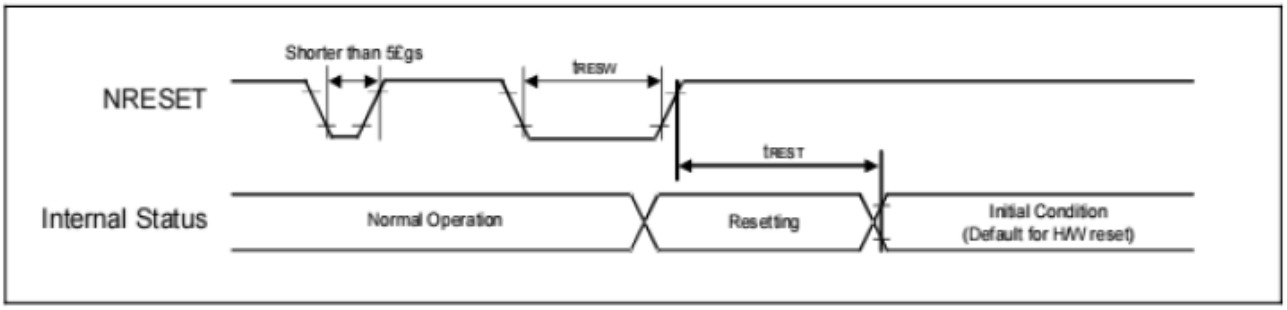
TCON (Embedded in Source IC) Input Timing (DCLK, HS, VS, DE)

VCI=3.3V, GND=0V, Ta=25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Fclk	-	49	-	MHz	
	tclk	-	20.4	-	ns	
HSD	thd	-	720	-	tclk	
	thpw	-	120	-	tclk	
	thb	-	120	-	tclk	
	thfp	-	120	-	tclk	
VSD	tvd	-	720	-	th	
	tvpw	-	4	-	th	
	tvb	-	16	-	th	
	tvfp	-	16	-	th	

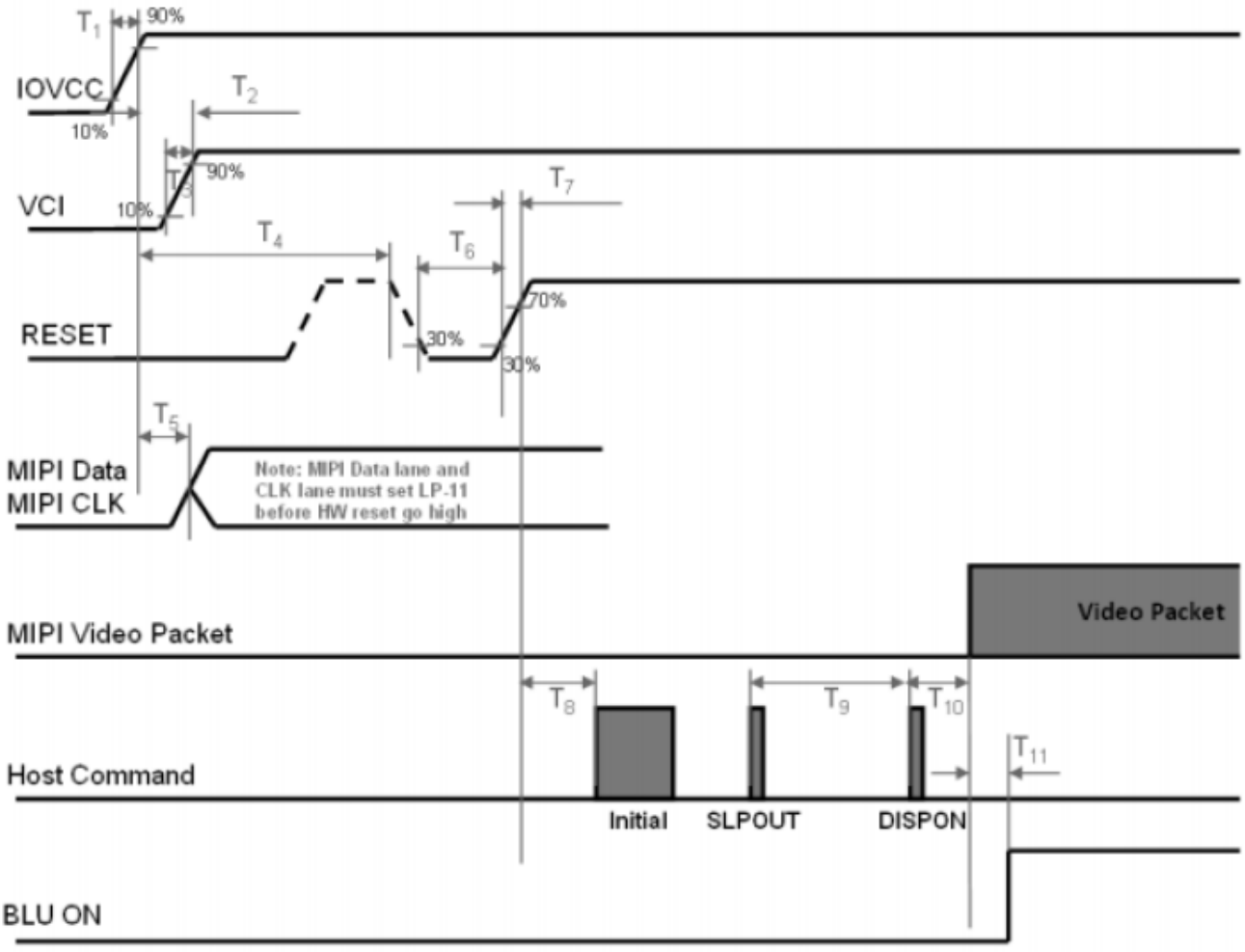
Note: For reference only, it needs to be adjusted according to the actual display effect.

5.3. Reset input timing



Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

5.4. Power On Sequence

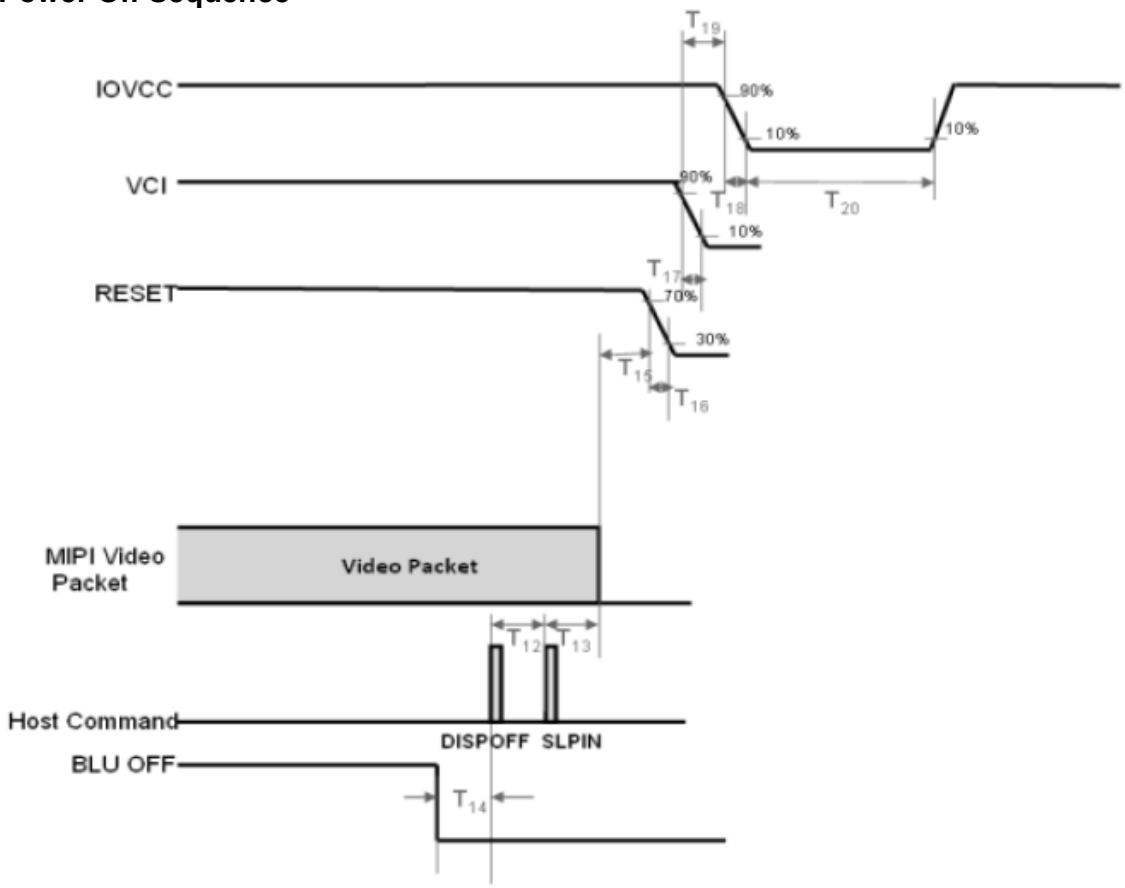


DSI Power On Sequence

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2	No Limit			ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7	No Limit			ns
T8	15	-	-	ms
T9	120	-	-	ms
T10	No Limit			ms
T11	100	150	-	ms

DSI Power On Timing

5.5. Power Off Sequence



DSI Power Off Sequence

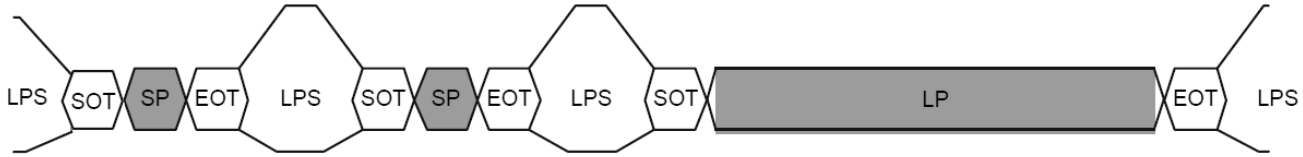
	Min.	Typ.	Max.	Unit
T12	2	-	-	Frame
T13	2	-	-	Frame
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	100			ms

DSI Power Off Timing

6.MIPI data input format(VESA)

6.1. DSI Packet Level Communication

The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure illustrates multiple HS Transmission packets.



LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

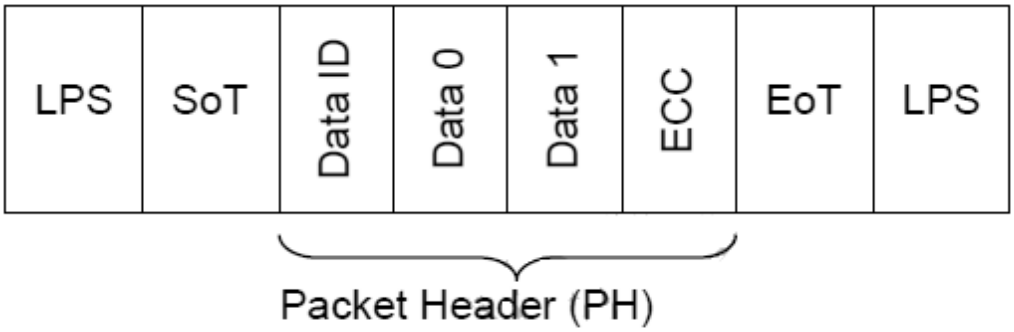
Figure 3: DSI multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

6.2. General Packet Structure

Short packets

Specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Below figure shows the structure of the Short packet.

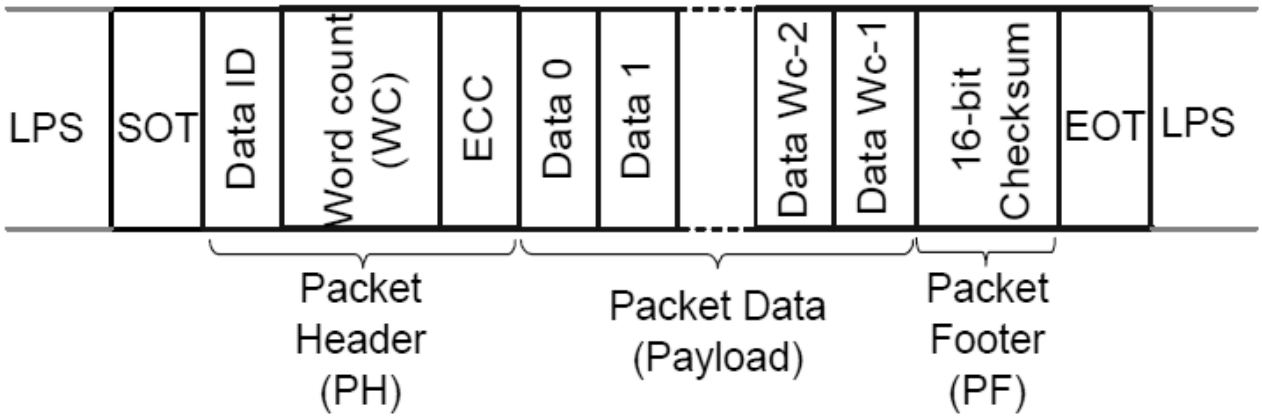


SOT: Start of Transmission
DI(Data ID): 8-bit Contain Virtual Channel Identifier and Data Type.
Data 0 and Data 1: Packet Data (8+8bit)
ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4: Structure of the short packet

Long packets

Specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Below figure shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.

WC (Word Count)：8+8 bits The receiver use WC to define packet end.

ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

PF(Packet Footer)：Mean 16-bit Checksum.

Figure 5: Structure of the long packet

7. Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	30	35	.ms	Note 3
Contrast ratio		CR	At optimized viewing angle	1000	1200	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.272	0.302	0.332	-	Note 2,5,6
		Wy		0.292	0.322	0.352	-	
Viewing angle (Gray Scale Inversion Direction)	Hor.	ΘR	CR≧10	80	85	-	Deg.	Note 1
		ΘL		80	85	-		
	Ver.	ΦT		80	85	-		
		ΦB		80	85	-		
Brightness		-	-	300	350	-	cd/m²	Center of display
Uniformity		(U)	-	70	-	-	%	Note 5

Ta=25±2℃,

Note 1: Definition of viewing angle range

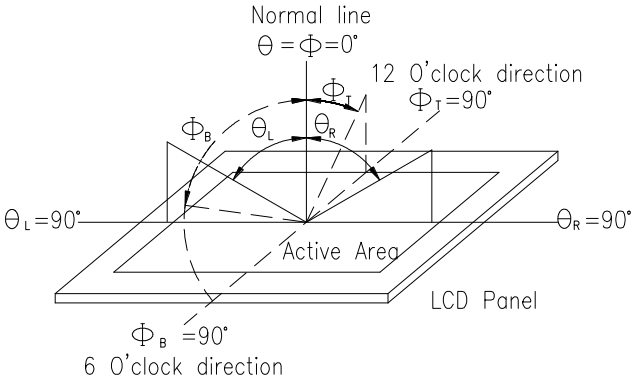


Fig. 8.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

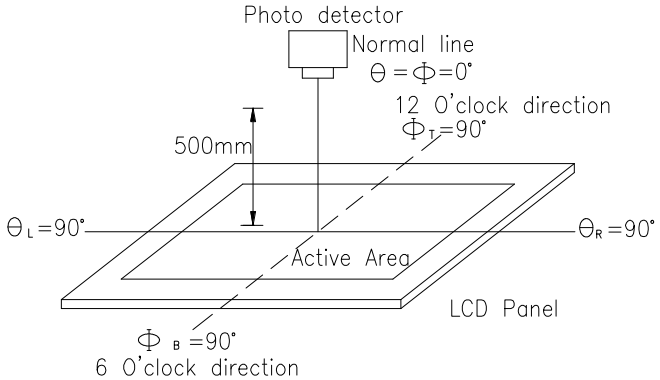
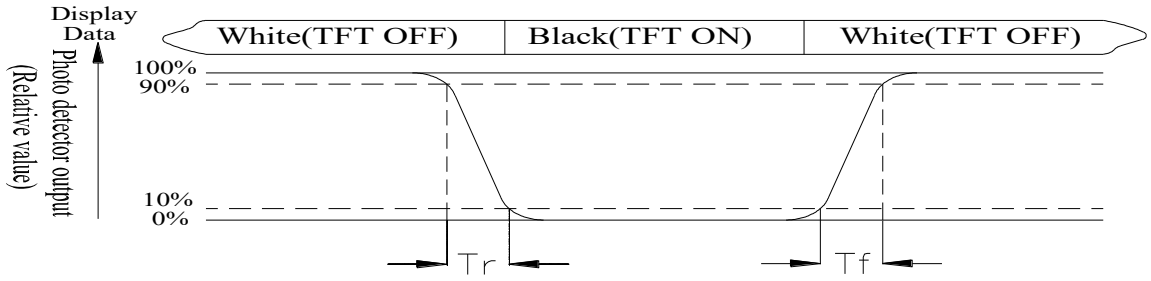


Fig. 7.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

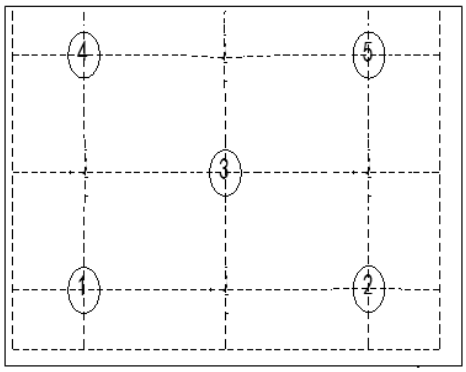


Fig7.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

8. Interface

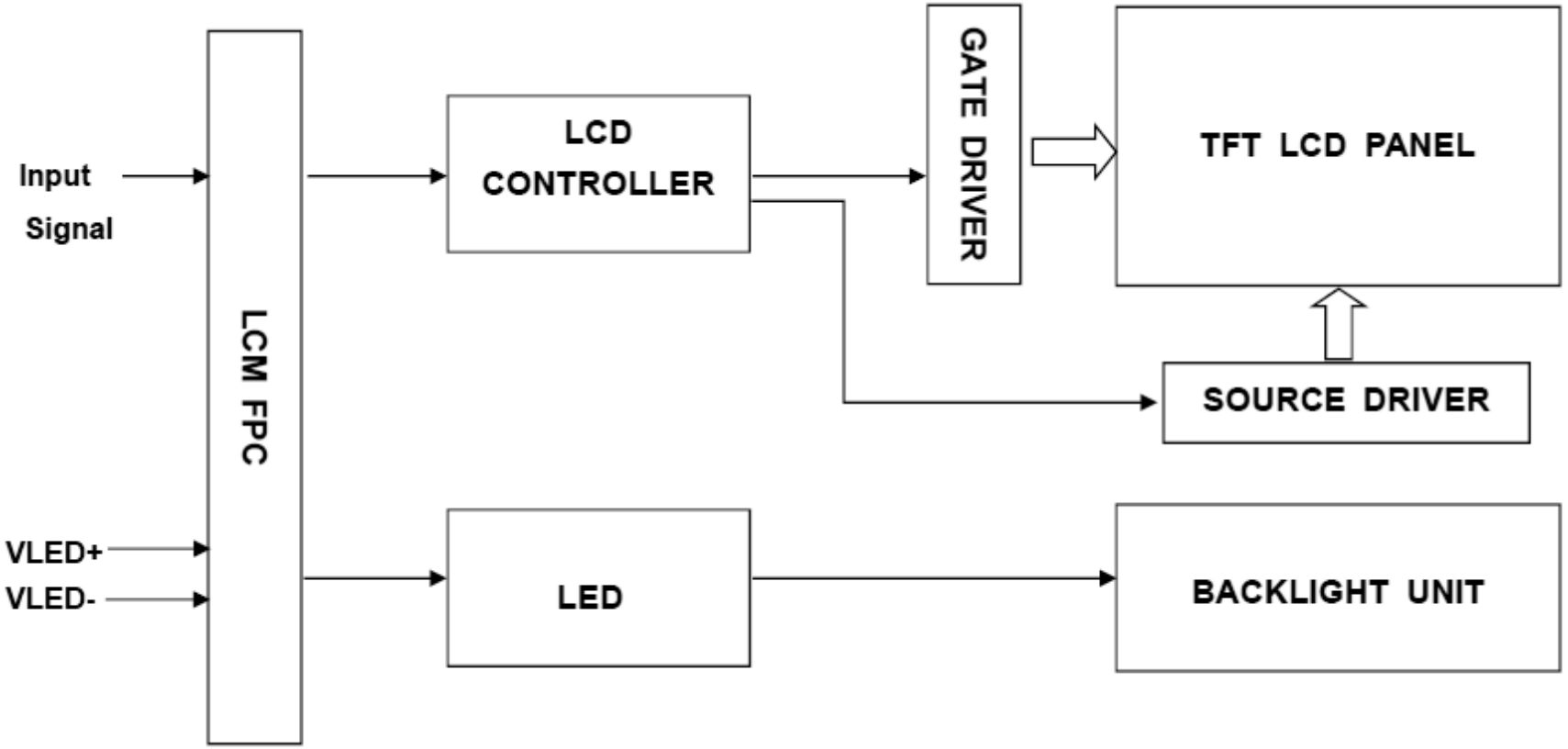
8.1. LCM PIN Definition

Match connector: XF2M-3015-1A（ OMRON ）or equivalent.

Pin No	Symbol	Description	Remark
1	VLED+	LED Anode	
2	VLED-	LED Cathode1	
3	VLED-	LED Cathode2	
4	VCI	Power Supply 2.8V	
5	IOVCC	LCD I/O power supply(1.8V)	
6	RESET	Reset pin	
7	TE	Tearing effect(1.8V)	
8	NC	No connection.	
9	GND	Ground	
10	D0P	MIPI DSI differential data pair (Data lane 0)	
11	D0N	MIPI DSI differential data pair (Data lane 0)	
12	GND	Ground	
13	D1P	MIPI DSI differential data pair (Data lane 1)	
14	D1N	MIPI DSI differential data pair (Data lane 1)	
15	GND	Ground	
16	CLKP	MIPI DSI differential clock pair	
17	CLKN	MIPI DSI differential clock pair	
18	GND	Ground	
19	D2P	MIPI DSI differential data pair (Data lane 2)	
20	D2N	MIPI DSI differential data pair (Data lane 2)	
21	GND	Ground	
22	D3P	MIPI DSI differential data pair (Data lane 3)	
23	D3N	MIPI DSI differential data pair (Data lane 3)	

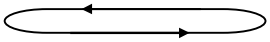
24	GND	Ground	
25-30	NC	No connection.	

9. Block Diagram



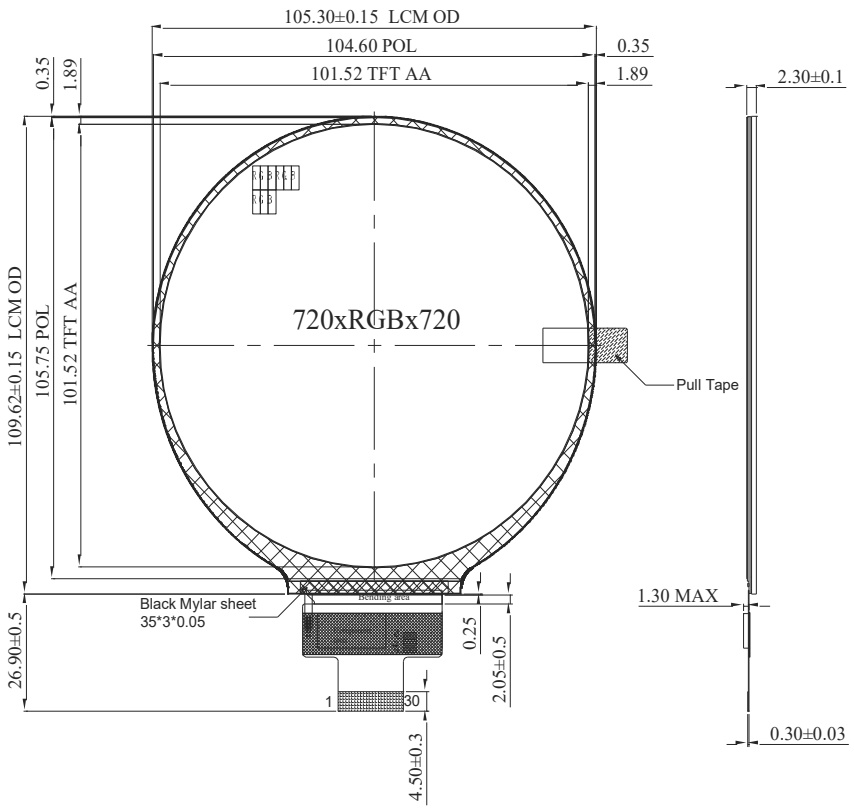
10.Reliability

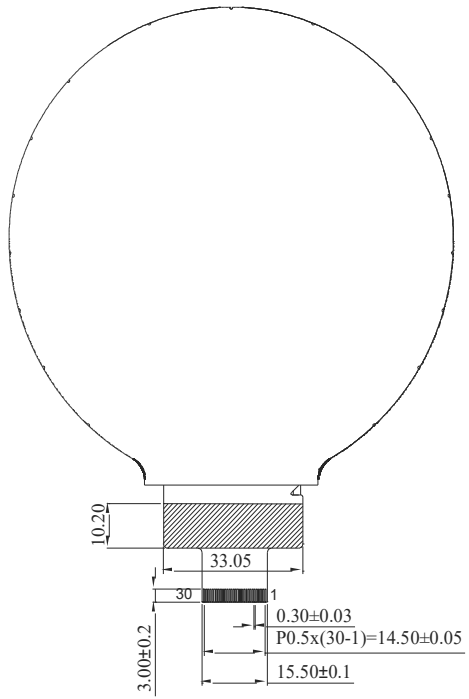
Content of Reliability Test (Wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 240hrs	1,2
High Temperature/ Humidity storage	The module should be allowed to stand at 60 ℃,90%RH max	60℃,90%RH 240hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of storage -30℃ 25℃ 70℃  30min 5min 30min 1 cycle	-30℃/70℃ 10 cycles	2
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±4KV(contact), ±6KV(air), RS=330Ω CS=150pF 5 times	4

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.
Note4: Endurance test applying the electric stress to the finished product housing

11.Contour Drawing





PIN	SYMBLE
1	VLED+
2	VLED-
3	VLED-
4	VCI
5	IOVCC
6	RESET
7	TE
8	NC
9	GND
10	D0P
11	D0N
12	GND
13	D1P
14	D1N
15	GND
16	CLKP
17	CLKN
18	GND
19	D2P
20	D2N
21	GND
22	D3P
23	D3N
24	GND
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC

The non-specified tolerance of dimension is ±0.3 mm .