ALL SHORE INDUSTRIES

# ASI-T-2201DA2SRN/D

| Item | Contents | Unit |
|---|---|---|
| Size | 2.2 | inch |
| Resolution | 240(RGB) x 320 | / |
| Interface | RGB + SPI | / |
| Color Depth | 262K dithering | / |
| Technology type | a-Si TFT | / |
| Pixel pitch | 0.141 x 0.141 | mm |
| Pixel Configuration | R.G.B. Vertical Stripe | |
| Outline Dimension (W x H x D) | 40.60 x 56.60 x 2.70 | mm |
| Active Area | 33.84 x 45.12 | mm |
| Display Mode | Transflective | / |
| Viewing Direction | 6 o'clock | / |
| Backlight Type | LED | / |
| Driver IC | ILI9341 | / |
| Weight | 11.8 (Typical) | g |

ALL SHORE INDUSTRIES

# Record of Revision

| Date | Revision No. | Summary |
|---|---|---|
| 2021-06-04 | 1.0 | Rev 1.0 was issued |
| | | |
| | | |

## 1. Scope

This data sheet is to introduce the specification of ASI-T-2201DA2SRN/D active matrix 262k color TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 2.2″ display area contains 240(RGB) x 320 pixels.

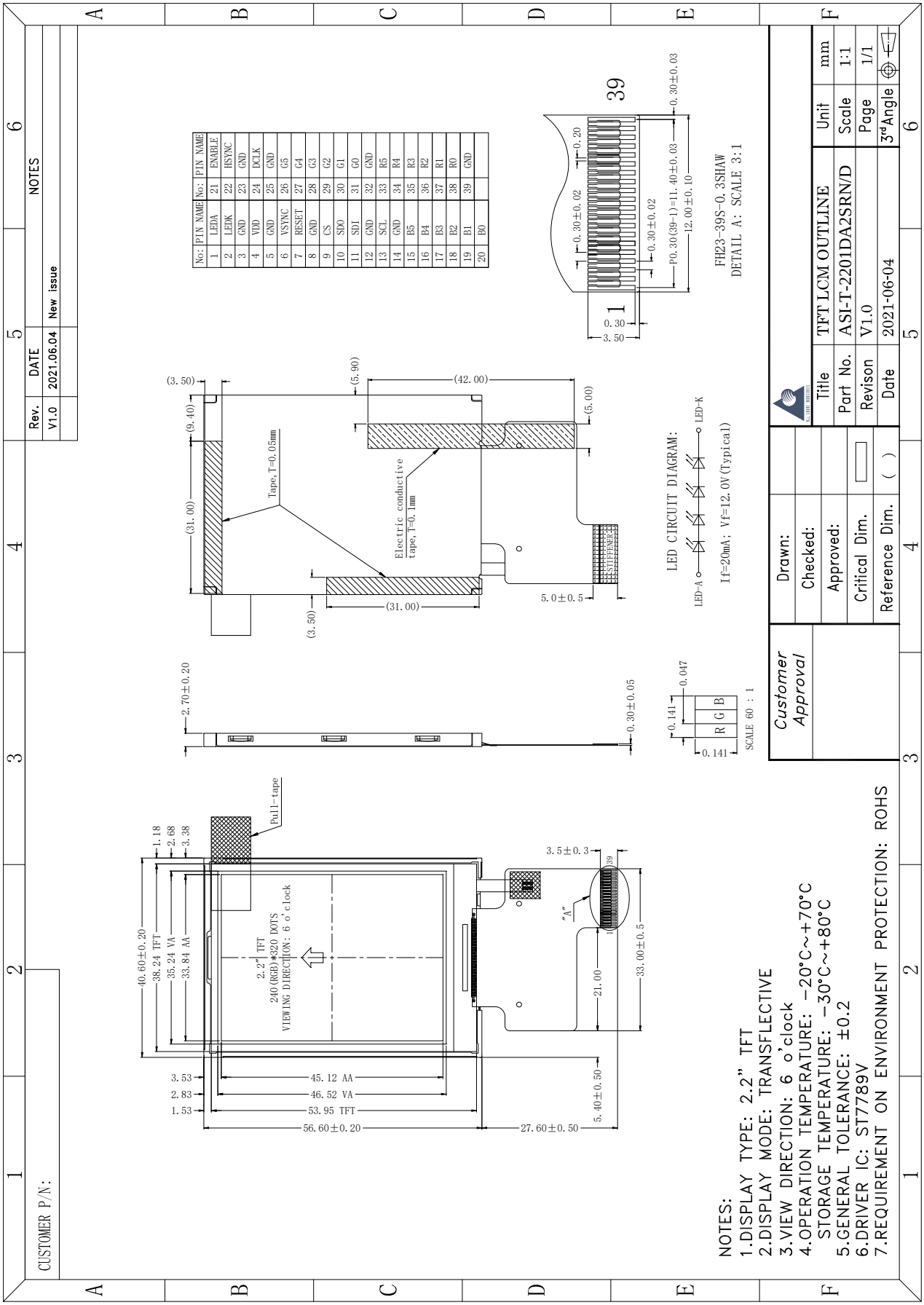
## 2. Application

Digital equipments which need color display outdoor, mobile navigator/video systems.

## 3. General Information

| Item | Contents | Unit |
|---|---|---|
| Size | 2.2 | inch |
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| Driver IC | ILI9341 | / |
| Weight | 11.8 (Typical) | g |

## 4. Outline Drawing




| No: | PIN NAME | No: | PIN NAME |
|---|---|---|---|
| 1 | LEDA | 21 | ENABLE |
| 2 | LEDK | 22 | HSYNC |
| 3 | GND | 23 | GND |
| 4 | VDD | 24 | DCLK |
| 5 | GND | 25 | GND |
| 6 | VSYNC | 26 | G5 |
| 7 | RESET | 27 | G4 |
| 8 | GND | 28 | G3 |
| 9 | CS | 29 | G2 |
| 10 | SDO | 30 | G1 |
| 11 | SDI | 31 | G0 |
| 12 | GND | 32 | GND |
| 13 | SCL | 33 | R5 |
| 14 | GND | 34 | R4 |
| 15 | B5 | 35 | R3 |
| 16 | B4 | 36 | R2 |
| 17 | B3 | 37 | R1 |
| 18 | B2 | 38 | R0 |
| 19 | B1 | 39 | GND |
| 20 | B0 | | |

## 5. Interface signals

| No | Symbol | Description | Remarks |
|---|---|---|---|
| 1 | LEDA | Power supply for LED(Anode) | |
| 2 | LEDK | Power supply for LED(Cathode) | |
| 3 | GND | Ground | |
| 4 | VDD | Power supply of analog | |
| 5 | GND | Ground | |
| 6 | VSYNC | Vertical sync. signal | |
| 7 | RESET | Reset Enable | |
| 8 | GND | Ground | |
| 9 | CS | SPI Chip select | |
| 10 | SDO | SPI serial Data output | |
| 11 | SDI | SPI serial Data input | |
| 12 | GND | Ground | |
| 13 | SCL | SPI serial interface clock | |
| 14 | GND | Ground | |
| 15 | B5 | Blue data signal | |
| 16 | B4 | Blue data signal | |
| 17 | B3 | Blue data signal | |
| 18 | B2 | Blue data signal | |
| 19 | B1 | Blue data signal | |
| 20 | B0 | Blue data signal | |
| 21 | ENABLE | Data enable signal | |
| 22 | HSYNC | Horizontal sync signal | |
| 23 | GND | Ground | |
| 24 | DCLK | Data sampling clock signal | |
| 25 | GND | Ground | |
| 26 | G5 | Green data signal | |
| 27 | G4 | Green data signal | |
| 28 | G3 | Green data signal | |

| | | | |
|---|---|---|---|
| 29 | G2 | Green data signal | |
| 30 | G1 | Green data signal | |
| 31 | G0 | Green data signal | |
| 32 | GND | Ground | |
| 33 | R5 | Red data signal | |
| 34 | R4 | Red data signal | |
| 35 | R3 | Red data signal | |
| 36 | R2 | Red data signal | |
| 37 | R1 | Red data signal | |
| 38 | R0 | Red data signal | |
| 39 | GND | Ground | |

Note: Corresponded connector:FH23-39S-0.3SHW

## 6. Absolute maximum Ratings

### 6.1. Electrical Absolute max. ratings

| Parameter | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Power Supply Voltage | VDD | -0.3 | 4.6 | V | |
| | VDDI | -0.3 | 4.6 | V | |

### 6.2. Environment Conditions

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Operating Temperature | TOPR | -20 | 70 | ℃ | |
| Storage Temperature | TSTG | -30 | 80 | ℃ | |

### 6.3. LED Backlight Absolute max. ratings

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Backlight Forward Current | ILED | -- | 25 | mA | |

# 7. Electrical Specifications

## 7.1 Electrical characteristics

GND=0V, Ta=25℃

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Supply Voltage for Logic | | VDD | 2.4 | 2.75 | 3.3 | V | |
| Input Signal Voltage | Low Level | VIL | VSS | -- | 0.3*VDDI | V | |
| | High Level | VIH | 0.7*VDDI | -- | VDDI | V | |
| Output Signal Voltage | Low Level | VOL | VSS | -- | 0.2*VDDI | V | |
| | High Level | VOH | 0.8*VDDI | -- | VDDI | V | |
| Input Current | | IDD | - | 7.2 | 10.8 | mA | |

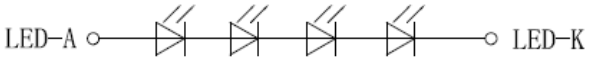
## 7.2 LED Backlight

Ta=25℃

| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | IF | -- | 20 | 25 | mA | 4LEDs serial |
| Forward Voltage | VF | -- | 12.0 | 13.6 | V | |
| Power Consumption | WBL | -- | 259.8 | -- | mW | |
| LED life time | -- | -- | 30,000 | -- | Hrs | |

Note: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED life time could be decreased if operating IL is large than 20mA.

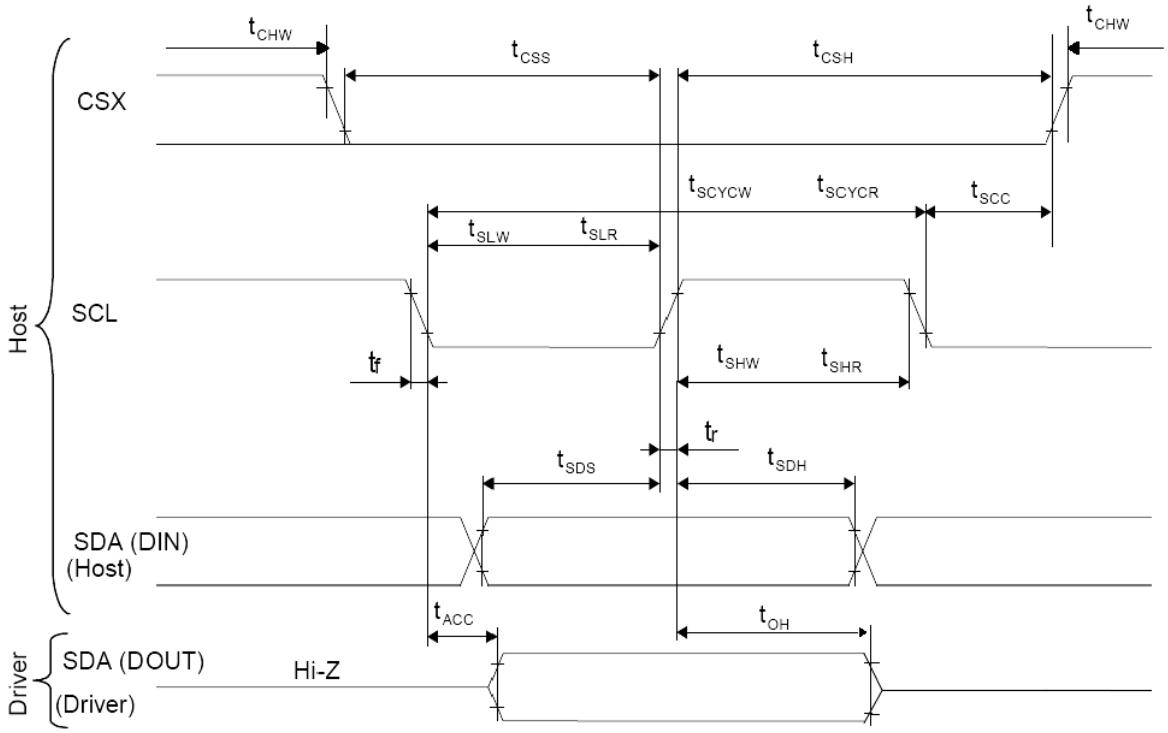
LED CIRCUIT DIAGRAM:




If=20mA; Vf=12.0V(Typical)

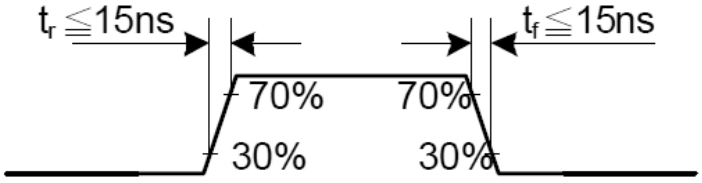
# 8. Command/AC Timing

## 8.1 Display Serial Interface Timing Characteristics (3-line SPI system)

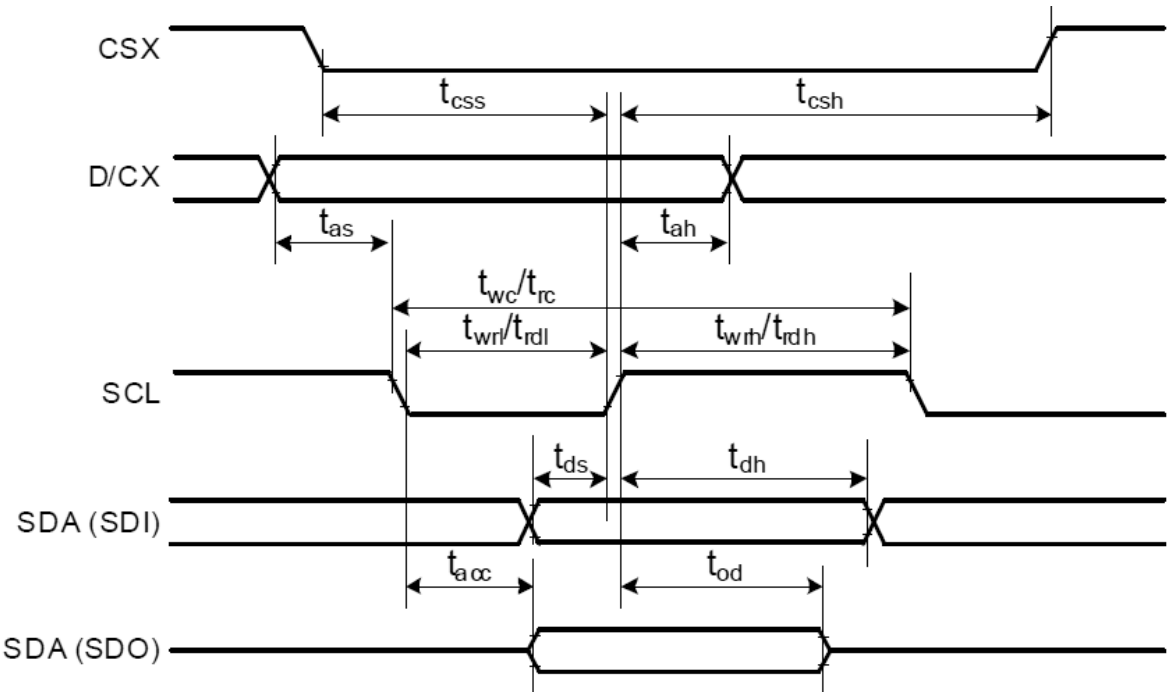



| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| SCL | tscycw | Serial clock cycle (write) | 100 | - | ns | |
| | tshw | SCL “H” pulse width (write) | 40 | - | ns | |
| | tslw | SCL “L” pulse width (write) | 40 | - | ns | |
| | tscycr | Serial clock cycle (read) | 150 | - | ns | |
| | tshr | SCL “H” pulse width (read) | 60 | - | ns | |
| | tslr | SCL “L” pulse width (read) | 60 | - | ns | |
| SDA/SDI (Input) | tsds | Data setup time (write) | 30 | - | ns | |
| | tsdh | Data hold time (write) | 30 | - | ns | |
| SDA/SDO (Output) | tacc | Access time (read) | 10 | - | ns | |
| | toh | Output disable time (read) | 10 | 50 | ns | |
| CSX | tscc | SCL-CSX | 20 | - | ns | |
| | tchw | CSX “H” pulse width | 40 | - | ns | |
| | tcss | CSX-SCL time | 60 | - | ns | |
| | tcsh | | 65 | - | ns | |

Note: Ta= 25℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, AGND=VSS= 0V.

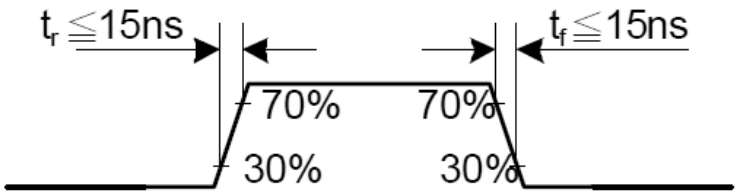


## 8.2 Display Serial Interface Timing Characteristics (4-line SPI system)

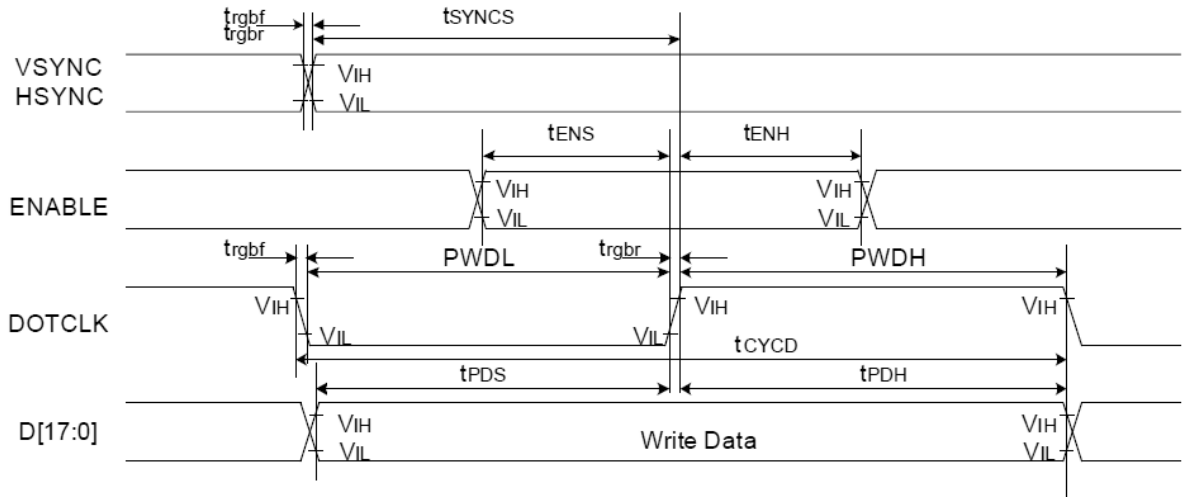



| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | tcss | Chip select time (write) | 40 | | | |
| | tcsh | Chip select hold time (read) | 40 | | | |
| SCL | twc | Serial clock cycle (write) | 100 | - | ns | |
| | twrh | SCL “H” pulse width (write) | 40 | - | ns | |
| | twrl | SCL “L” pulse width (write) | 40 | - | ns | |
| | trc | Serial clock cycle (read) | 150 | - | ns | |
| | trdh | SCL “H” pulse width (read) | 60 | - | ns | |
| | trdl | SCL “L” pulse width (read) | 60 | - | ns | |
| D/CX | tas | D/CX setup time | 10 | - | | |
| | tah | D/CX hold time (write/read) | 10 | - | | |
| SDA/SDI (Input) | tds | Data setup time (write) | 30 | - | ns | |
| | tdh | Data hold time (write) | 30 | - | ns | |
| SDA/SDO (Output) | tacc | Access time (read) | 10 | - | ns | For maximum CL=30pF<br>For minimum CL=8pF |
| | tod | Output disable time (read) | 10 | 50 | ns | |

Note: Ta= 25℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, AGND=VSS= 0V.

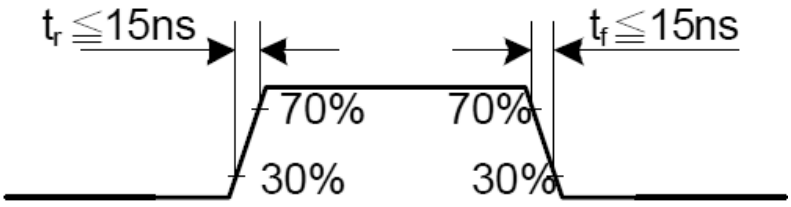


## 8.3 Parallel 18/16/6-bit RGB Interface Timing Characteristics




| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| VSYNC/ HSYNC | tSYNCS | VSYNC/HSYNC setup time | 15 | - | | 18/16-bit bus RGB Interface mode |
| | tSYNCH | VSYNC/HSYNC hold time | 15 | - | | |
| DE | tENS | DE setup time | 15 | - | | |
| | tENH | DE hold time | 15 | - | | |
| D[17:0] | tPOS | Data setup time | 15 | - | | |
| | tPDH | Data hold time | 15 | - | | |
| DOTCLK | PWDH | DOTCLK high-level period | 15 | - | ns | |
| | PWDL | DOTCLK low-level period | 15 | - | ns | |
| | tCYCD | DOTCLK cycle time | 100 | - | | |
| | trgbr, trgbf | DOTCLK,HSYNC,VSYNC rise/fall time | - | 15 | | |
| VSYNC/ HSYNC | tSYNCS | VSYNC/HSYNC setup time | 15 | - | ns | 6-bit bus RGB Interface mode |
| | tSYNCH | VSYNC/HSYNC hold time | 15 | - | ns | |
| DE | tENS | DE setup time | 15 | - | ns | |
| | tENH | DE hold time | 15 | - | ns | |
| D[17:0] | tPOS | Data setup time | 15 | - | ns | |
| | tPDH | Data hold time | 15 | - | ns | |
| DOTCLK | PWDH | DOTCLK high-level period | 15 | - | ns | |
| | PWDL | DOTCLK low-level period | 15 | - | ns | |
| | tCYCD | DOTCLK cycle time | 50 | - | ns | |
| | trgbr, trgbf | DOTCLK,HSYNC,VSYNC rise/fall time | - | 15 | ns | |

Note: Ta= -30 to 70℃, VDDI= 1.65V to 3.3V, VCI= 2.5V to 3.3V, AGND=VSS= 0V.



## 8.4 Reset Timings

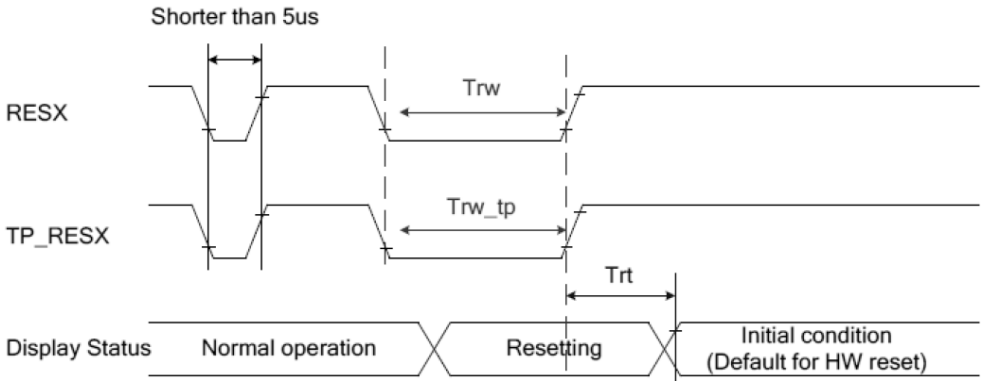



Figure: Reset Timing

| Signal | Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| RESX | Trw | Reset pulse duration | 10 | - | us |
| | Trt | Reset cancel | 35(Note1,5) | - | ms |
| | | | 150(Note1,6,7) | - | ms |
| TP_RESX | Trt_tp | Reset pulse duration | 1 | - | us |

Table: Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other setting from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

| RESX | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts in sleep out mode. The display remains the blank state in sleep in mode.) and return to default condition for hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

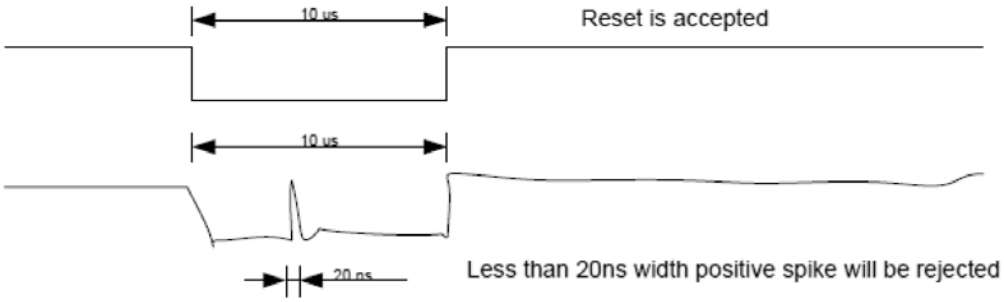



Figure: Positive Noise Pulse during Reset Low

5. When Reset applied during sleep in mode.
6. When Reset applied during sleep out mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also sleep out command (11h) cannot be sent for 120msec.

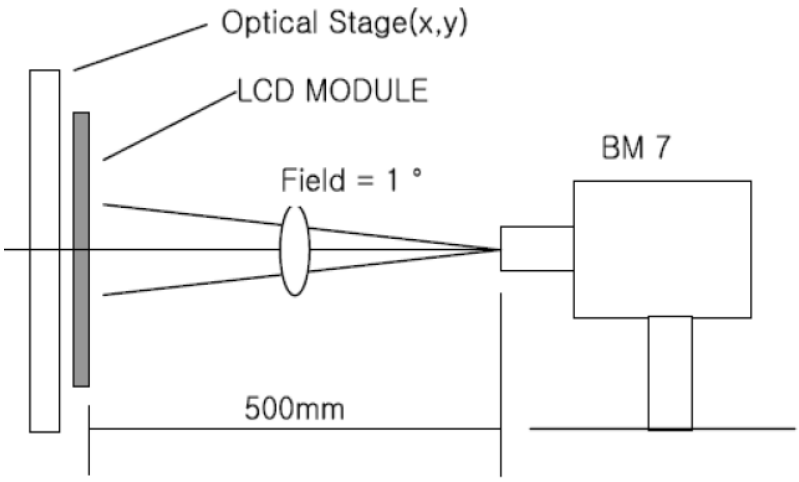
## 9. Optical Specification

| Item | | Symbol | Condition | Min | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | θ=0° | 20 | 50 | - | | Note1<br>Note3 |
| Response Time | | Ton/ Toff | 25℃ | - | 35 | 50 | ms | Note1<br>Note4 |
| View Angles | | ΘT | CR≧10 | - | 15 | - | Degree | Note 2 |
| | | ΘB | | - | 80 | - | | |
| | | ΘL | | - | 25 | - | | |
| | | θR | | - | 10 | - | | |
| Chromaticity | White | x | Brightness is on | Typ-0.05 | 0.3262 | Typ+0.05 | | Note5, |
| | | y | | | 0.3279 | | | |
| | Red | x | | | 0.6337 | | | |
| | | y | | | 0.3321 | | | |
| | Green | x | | | 0.3950 | | | |
| | | y | | | 0.3486 | | | |
| | Blue | x | | | 0.1018 | | | |
| | | y | | | 0.1393 | | | |
| Luminance | | L | | 160 | 210 | - | cd/m$^2$ | Note6 |
| Uniformity | | | | 70 | - | - | % | Note7 |
| NTSC | | | | - | 40 | - | % | |

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

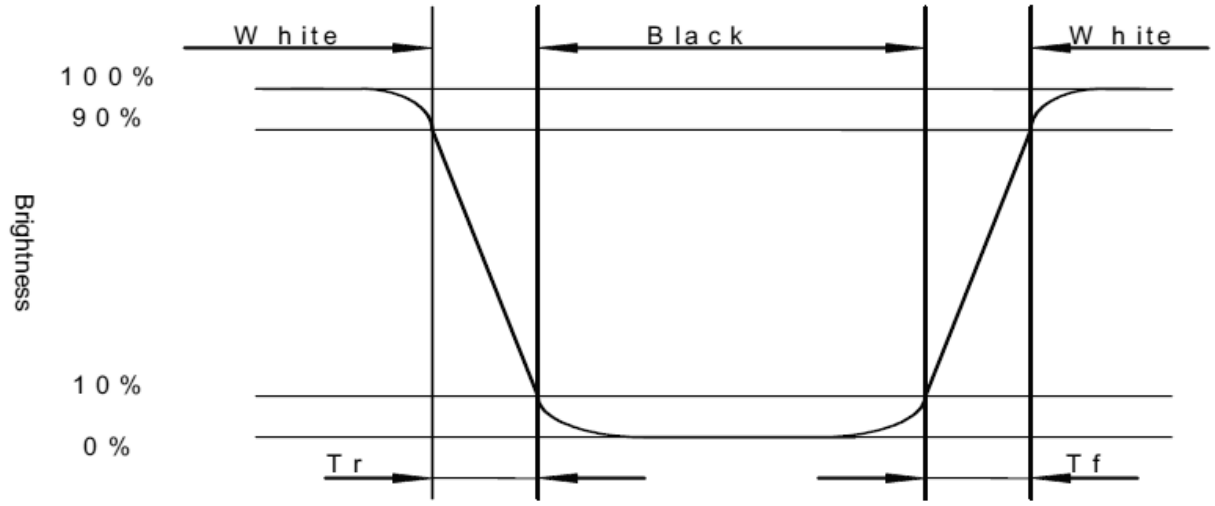



Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

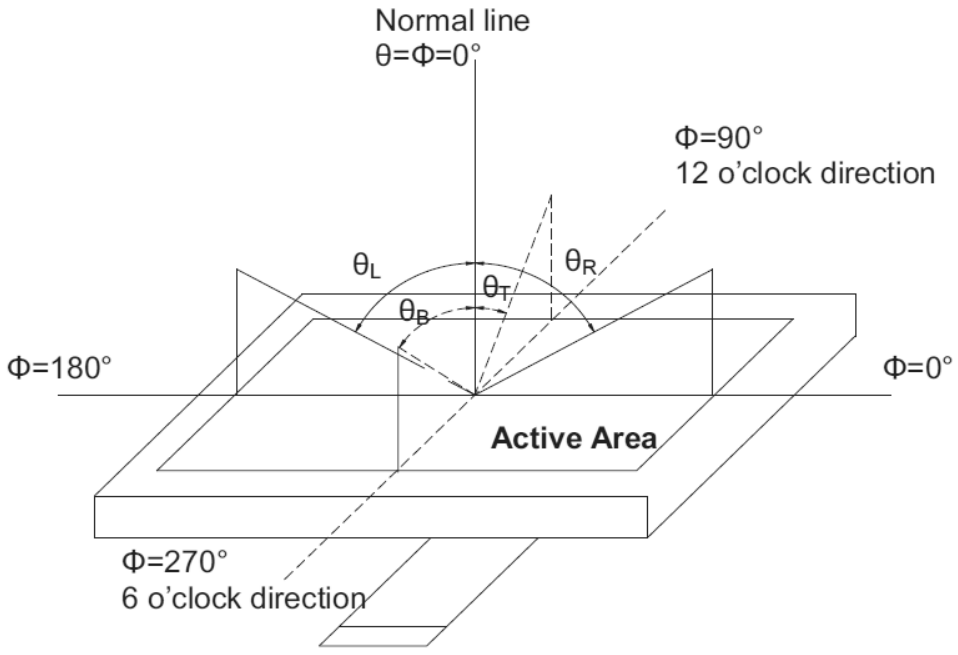
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



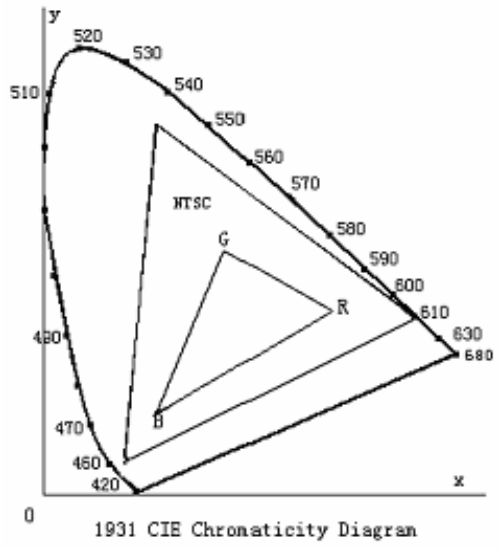

Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.




Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.




$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

## Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

## Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance( brightness ) in 9 points}}{\text{Maximum Luminance( brightness ) in 9 points}}$$

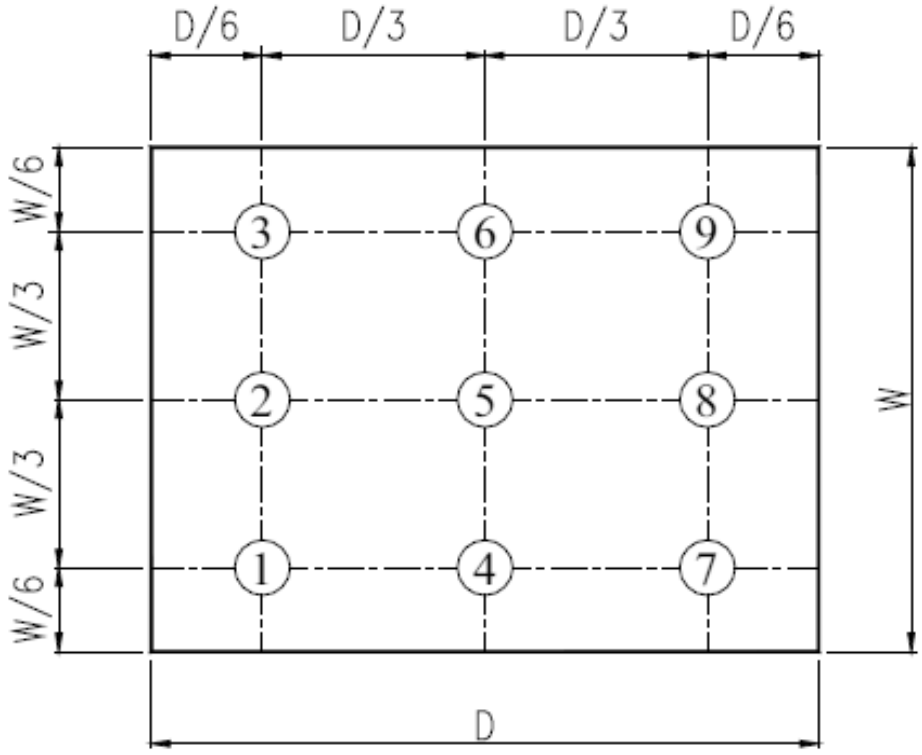



Fig. 2 Definition of uniformity

## 10. Environmental / Reliability Tests

| No | Test Item | Condition | Judgment criteria |
|---|---|---|---|
| 1 | High Temp Operation | Ta=+70℃, 120hrs | Per table in below |
| 2 | Low Temp Operation | Ta=-20℃, 120hrs | Per table in below |
| 3 | High Temp Storage | Ts=+80℃, 120hrs | Per table in below |
| 4 | Low Temp Storage | Ts=-30℃, 120hrs | Per table in below |
| 5 | High Temp & High Humidity Storage | Ts=+50℃, 90% RH, 120 hours | Per table in below (polarizer discoloration is excluded) |
| 6 | Thermal Shock (Non-operation) | -30℃ 30 min~+80℃ 30 min, Change time:5min, 10 Cycles | Per table in below |
| 7 | ESD (Operation) | C=150pF, R=330Ω， 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; | Per table in below |
| 8 | Vibration (Non-operation) | Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. | Per table in below |
| 9 | Package Drop Test | Height:80 cm, 1 corner, 3 edges, 6 surfaces | Per table in below |

| INSPECTION | CRITERION(after test) |
|---|---|
| Appearance | No Crack on the FPC, on the LCD Panel |
| Alignment of LCD Panel | No Bubbles in the LCD Panel<br>No other Defects of Alignment in Active area |
| Electrical current | Within device specifications |
| Function / Display | No Broken Circuit, No Short Circuit or No Black line<br>No Other Defects of Display |

# 11. Precautions for Use of LCD Modules

## 11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

## 11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

## 11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

## 11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

## 11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

## 11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, ASI recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.

