



ASI-T-1010JA3AN/D

Item	Contents	Unit
Size	10.1	inch
Resolution	1024 (RGB) x 600	/
Interface	RGB	/
Technology type	a-Si TFT	/
Pixel pitch	0.2175x0.2088	mm
Pixel Configuration	RGB stripes	
Outline Dimension (W x H x D)	235.0x143.0x5.1	mm
Active Area	222.72 x 125.28	mm
Display Mode	Normally white, Transmissive	/
Backlight Type	LED	/
Weight	TBD	g

1. Scope

This data sheet is to introduce the specification of ASI-T-1010JA3AN/D active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 10.1" display area contains 1024(RGB) x 600 pixels.

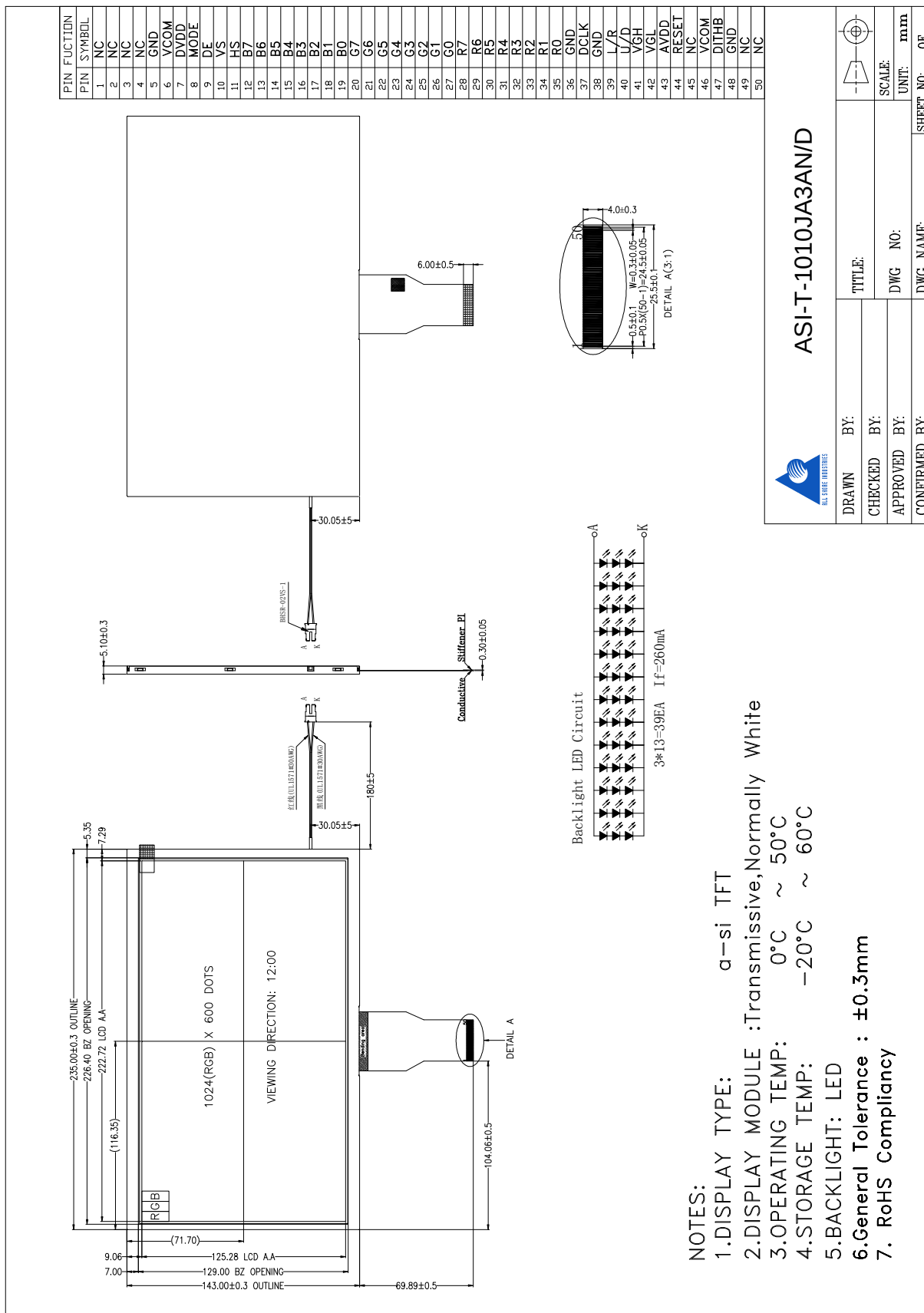
2. Application

Digital equipments which need color display, mobile navigator/video systems, tablet/notebook.

3. General Information

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4. Outline Drawing



5. Interface signals

Recommend connector:FH12S-50S-0.5SH

No	Symbol	Description	Remarks
1	NC	No Connection(Reserve)	
2	NC	No Connection(Reserve)	
3	NC	No Connection(Reserve)	
4	NC	No Connection(Reserve)	
5	GND	Power ground	
6	VCOM	Common voltage	
7	DVDD	Digital power	
8	MODE	DE/SYNC mode select	
9	DE	Data input enable	
10	VS	Vertical sync input	
11	HS	Horizontal sync input	
12	B7	Blue data (MSB)	
13	B6	Blue data	
14	B5	Blue data	
15	B4	Blue data	
16	B3	Blue data	
17	B2	Blue data	
18	B1	Blue data	
19	B0	Blue data (LSB)	
20	G7	Green data (MSB)	
21	G6	Green data	
22	G5	Green data	
23	G4	Green data	
24	G3	Green data	
25	G2	Green data	
26	G1	Green data	
27	G0	Green data (LSB)	
28	R7	Red data(MSB)	
29	R6	Red data	
30	R5	Red data	
31	B4	Red data	
32	R3	Red data	
33	R2	Red data	
34	R1	Red data	
35	R0	Red data (LSB)	
36	GND	Power ground	
37	DCLK	Clock input	
38	GND	Power ground	
39	L/R	Left or Right display control	
40	U/D	Up or Down display control	
41	VGH	Positive power for TFT	

42	VGL	Negative power for TFT	
43	AVDD	Analog power	
44	RSTB	Global reset pin	
45	NC	No Connection(Reserve)	
46	VCOM	Common voltage	
47	DITHB	Dithering function	
48	GND	Power ground	
49	NC	No Connection(Reserve)	
50	NC	No Connection(Reserve)	

Note1: DE/SYNC mode select, Normally pull high
 When MODE=H, DE mode
 When MODE=L, SYNC mode

Note2: source driver internal shift register is controlled by this pin as shown below
 Normally pull high

Note 3: Gate driver UP/DOWN scan setting, Normally pull low
 When U/D=H, reverse scan.
 STV1 output vertical start pulse and UD pin output "H" to gate driver
 When U/D=L, normal scan (default)
 STV2 output vertical start pulse and UD pin output "L" to gate driver

Note 4: Dithering function enable control, Normally pull low
 When DITHB=H, Enable internal dithering function
 When DITHB=L, Disable internal dithering function

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Digital Supply Voltage	DVDD	-0.3	5.0	V	
TFT Gate on voltage	VGH	-0.3	40	V	
TFT Gate off voltage	VGL	-20	0.3	V	
Analog power supply voltage	AVDD	-0.5	15	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	0	50	°C	
Storage Temperature	TSTG	-20	60	°C	

6.3. LED Backlight Absolute max. ratings

Item	Symbol	MIN	MAX	Unit	Remark
Forward current	I _{LED}	-	25	mA	For each LED

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Digital Supply Voltage	DVDD	3.0	3.3	3.6	V	
TFT Gate on voltage	VGH	20	21	22	V	
TFT Gate off voltage	VGL	-6.5	-5.5	-4.5	V	
Analog power supply voltage	AVDD	10.65	10.85	11.05	V	
TFT Common electrode voltage	VCOM	3.6	3.8	4.0	V	

7.2 LED Backlight

Ta=25°C

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	260	-	mA	Between A and K in below circuit.
Forward Voltage	VF	-	9.6	-	V	
LED lifetime	-	-	25,000	-	Hrs	

8. Command/AC Timing

8.1 Timing Conditions

INPUT SIGNAL TIMING

1AC ELECTRICAL CHARACTERISTICS

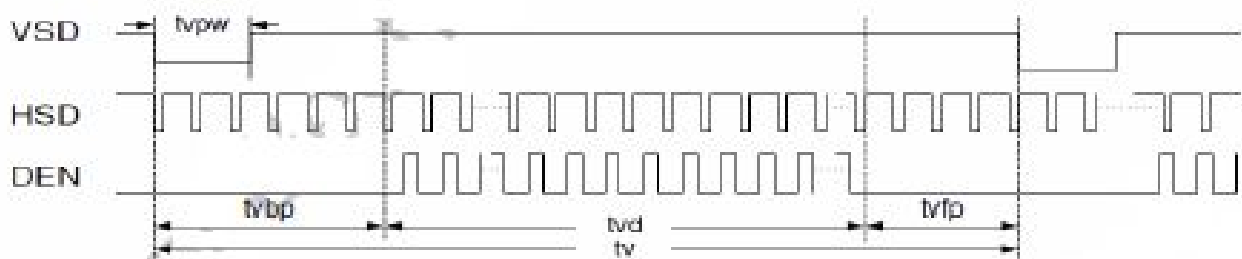
1. 1. TTL Mode AC Electrical Characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VDD Power On Slew rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB pulse width	T_{Rst}	50	-	-	us	DCLK=65MHz
DCLK cycle time	T_{cph}	14	-	-	ns	
DCLK pulse duty	T_{cwh}	40	50	60	%	
VSD setup time	T_{vst}	5	-	-	ns	
VSD hold time	T_{vhd}	5	-	-	ns	
HSD setup time	T_{hst}	5	-	-	ns	
HSD hold time	T_{hhd}	5	-	-	ns	
Data set-up time	T_{dsu}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	T_{dhd}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	T_{esu}	5	-	-	ns	
DE hold time	T_{ehd}	5	-	-	ns	
Output stable time	T_{sst}	-	-	6	us	10% to 90% target voltage.CL=90pF, R=10K ohm(Cascade)
				3		Dual gate

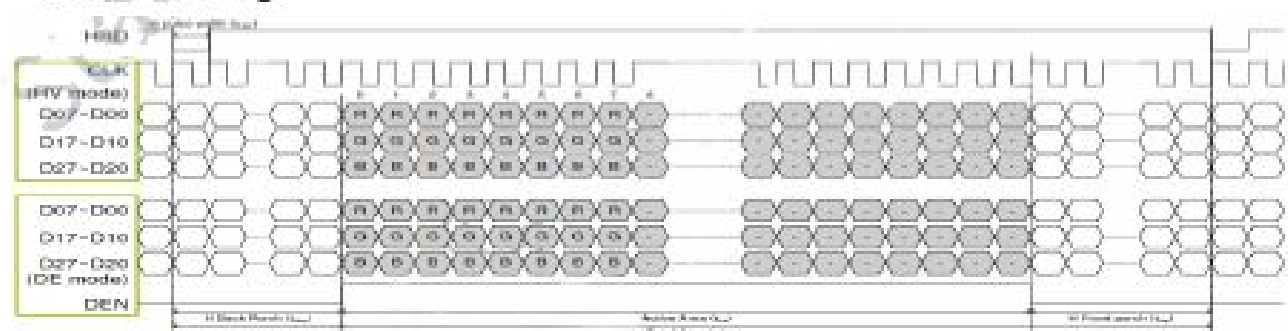
DATA INPUT FORMAT

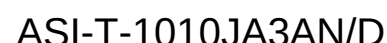
TTL Mode Data Input Format

Vertical Timing



Horizontal Timing





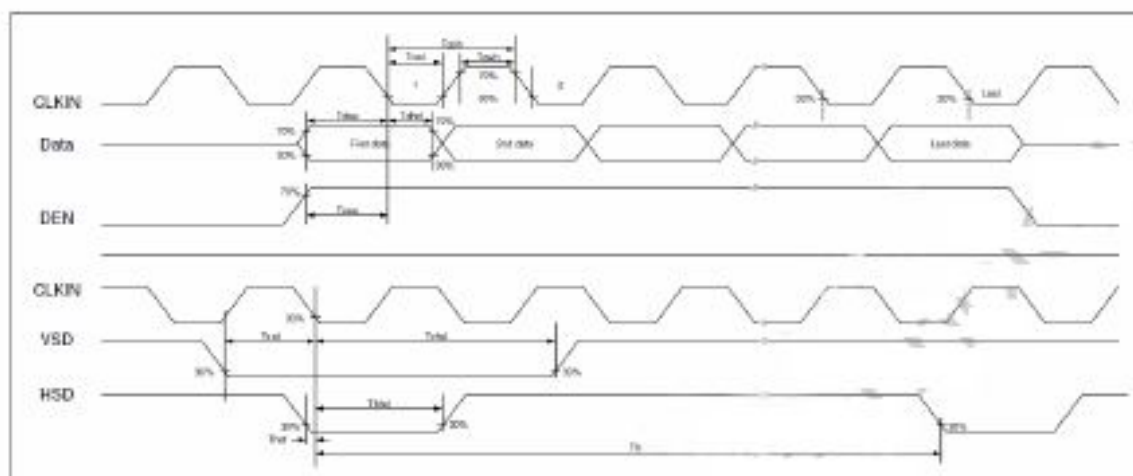
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd	600			TH
VSD Period	tv	610	635	800	TH
VSD Blanking	tvbp+ tvfp	10	35	200	TH

Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp	160			DCLK
HSD Front Porch	thfp	16	160	216	DCLK

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd	600			TH
VSD Period	tv	624	635	750	TH
VSD Pulse Width	tvpw	1	-	20	TH
VSD Back Porch	tvbp	23			TH
VSD Front Porch	tvfp	1	12	127	TH

1 Input Clock and Data Timing Diagram

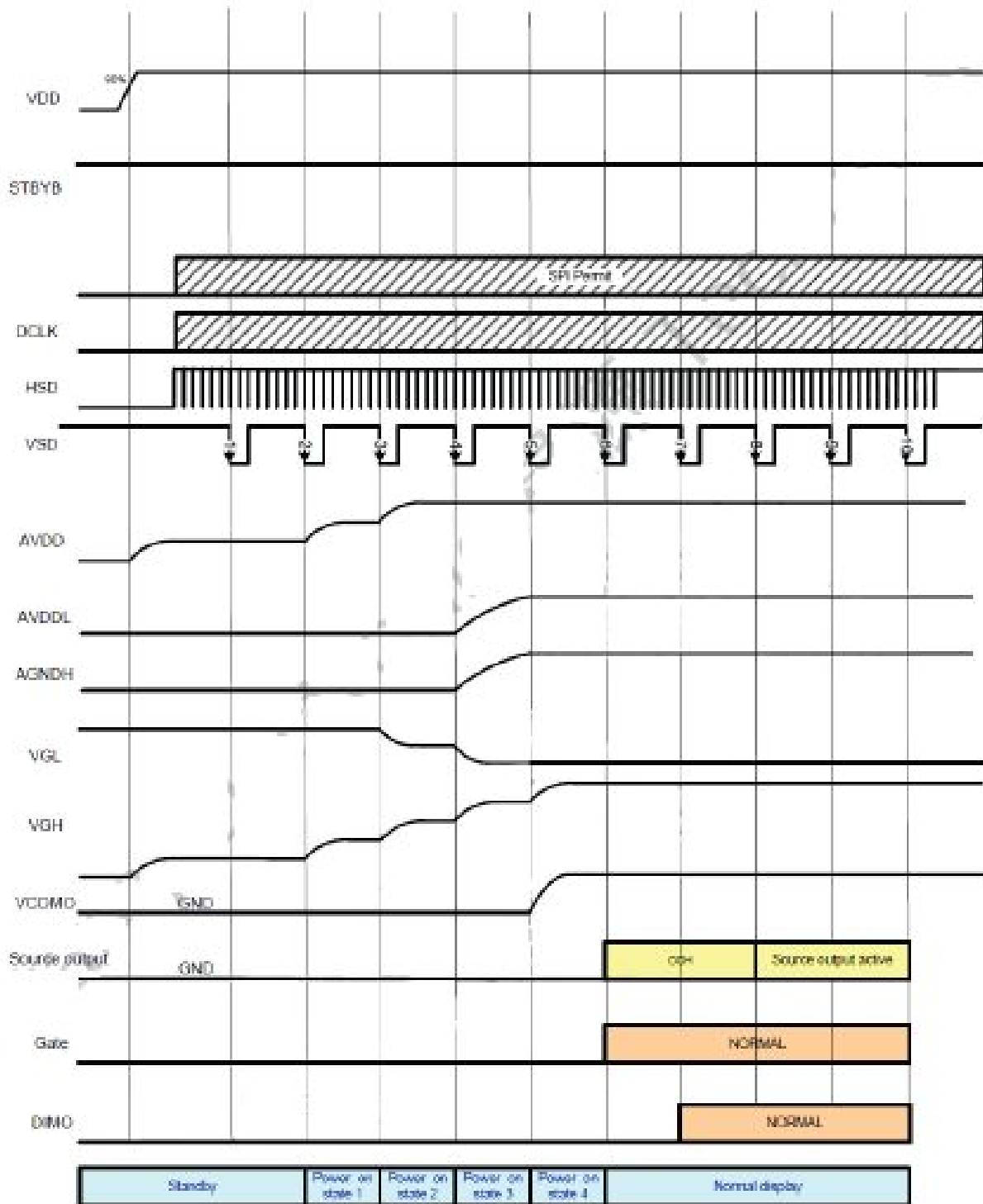


8.2 Power Sequence

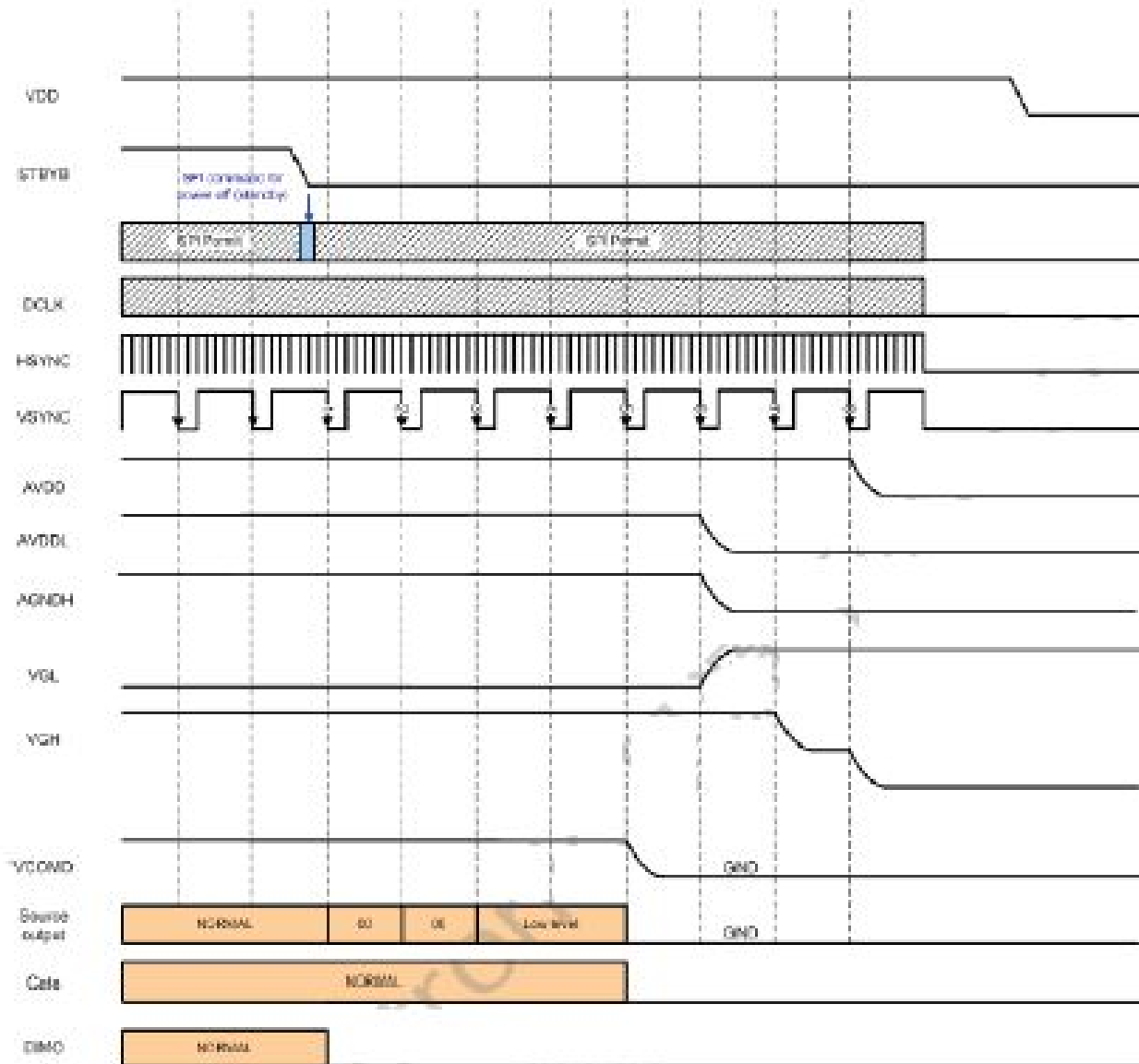
To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14

Power off: V1 to V14 → AVDD, AGND → VDD, GND



Power on timing sequence



Power off timing sequence

Note: Low level=3FH, when NBW=L (Normally white)

Low level=00H, when NBW=H (Normally black)

9. Optical Specification

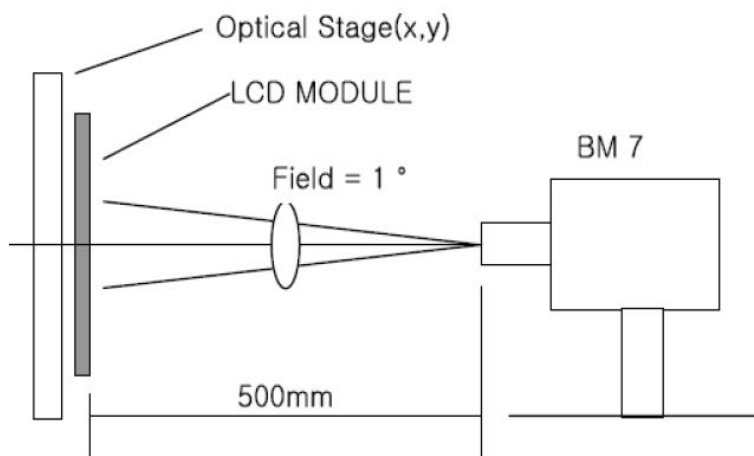
Ta=25°C

Item	Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	$\theta=0^\circ$	320	400	-		Note1 Note2
Response Time	Tr+Tf	25°C	-	25	40	ms	Note1 Note3
View Angles	θT	$CR \geq 10$	55	65	-	Degree	Note 4
	θB		65	75	-		
	θL		50	60	-		
	θR		50	60	-		
Chromaticity	White	Brightness is on	x	0.28	0.31	0.35	Note5, Note1
			y	0.29	0.33	0.36	
Luminance	L		-	380	-	cd/m ²	Note1 Note6
Uniformity	U		70	75	-	%	Note1 Note7

Note 1: Definition of optical measurement system.

Temperature = 25°C (±3°C)

LED back-light: ON, Environment brightness < 150 lx

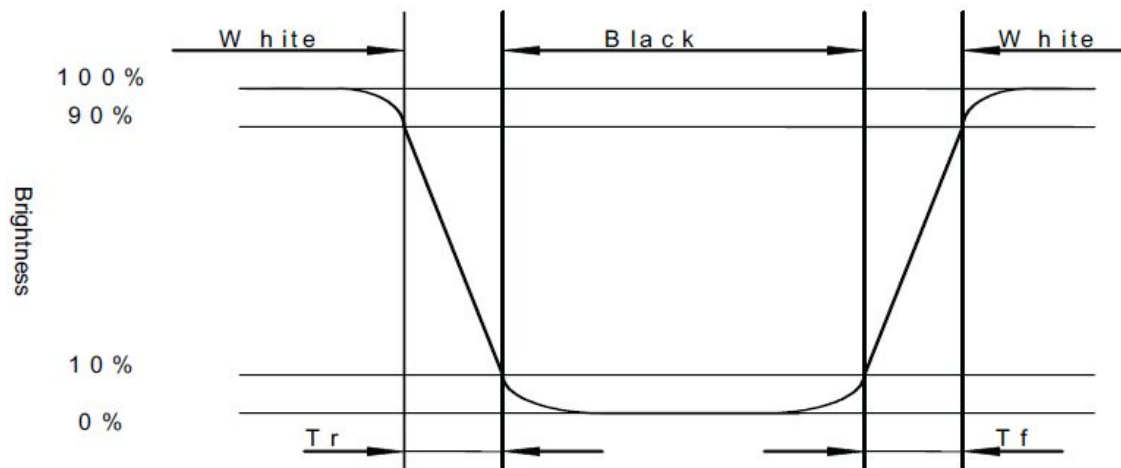


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

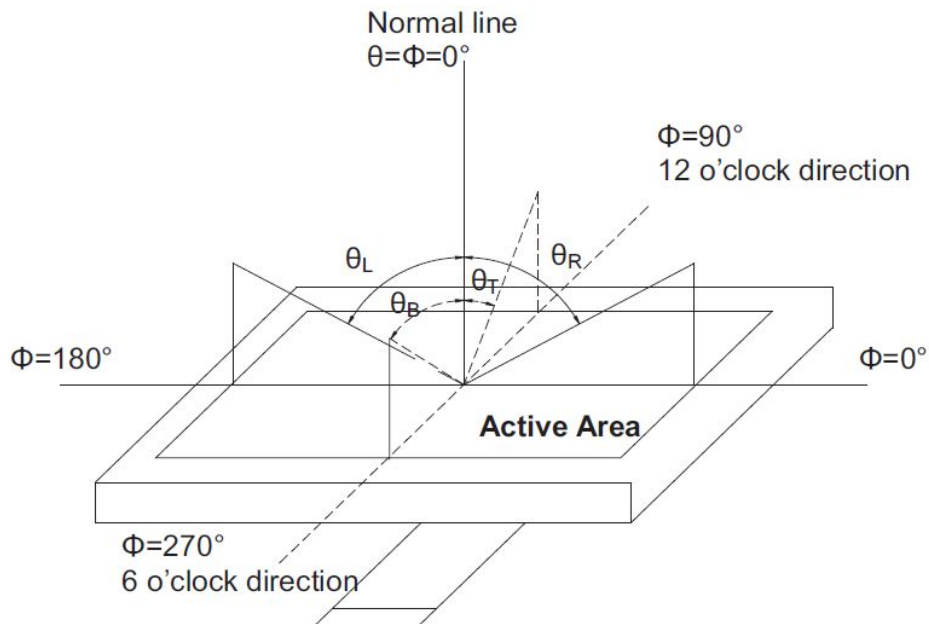
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, T_r) and from white to black (Decay Time, T_f).



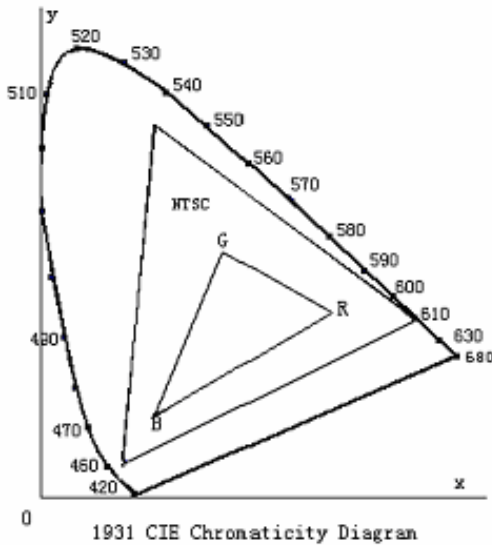
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

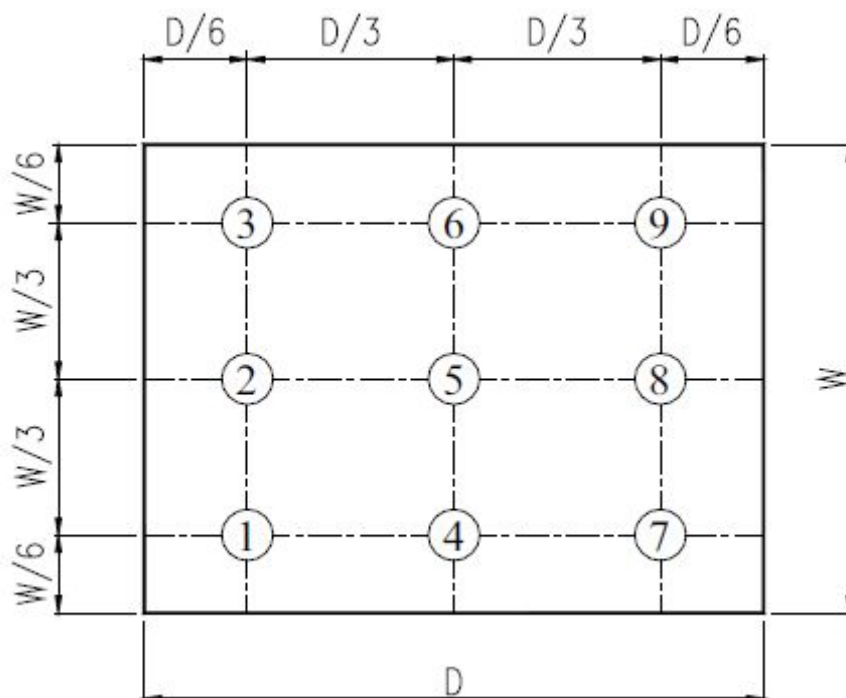


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+50, 120hrs	Per table in below
2	Low Temp Operation	Ta=0°C, 120hrs	Per table in below
3	High Temp Storage	Ta=+60°C, 120hrs	Per table in below
4	Low Temp Storage	Ta=-20°C, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60°C, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-20°C 30 min~+60°C 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω , 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

- A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
- C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- D. Provide a space so that the panel does not come into contact with other components.
- E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
- G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
- H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

- A. Ground soldering iron tips, tools and testers when they are in operation.
- B. Ground your body when handling the products.
- C. Power on the LCD module before applying the voltage to the input terminals.
- D. Do not apply voltage which exceeds the absolute maximum rating.
- E. Store the products in an anti-electrostatic bag or container.

11.4 Storage

- A. Store the products in a dark place at $+25^{\circ}\text{C} \pm 10^{\circ}\text{C}$ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

- A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

