

ASI-O-146GAFFF80/M

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	65K/262K	-
3	Duty	1/128	-
4	Resolution	128(H) x 128(V)	Pixel
5	Active Area	26.279 (W) x 26.284 (H)	mm^2
6	Outline Dimension	33.50 (W) x 33.50 (H) x 1.61 (D)	mm ³
7	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm^2
8	Dot Size	0.0435 (W) x 0.1855 (H)	mm^2
9	Aperture Rate	57	%
10	Driver IC	SSD1351	-
11	Interface	8/16/18-bit 6800/8080-series parallel, SPI	-
12	Weight	3.93±10%	g



REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2013-05-24	First Release	
2.0	2014-05-21	Old Part # ASI-O-14612812IS-OQ-F-S/M	





CONTENT

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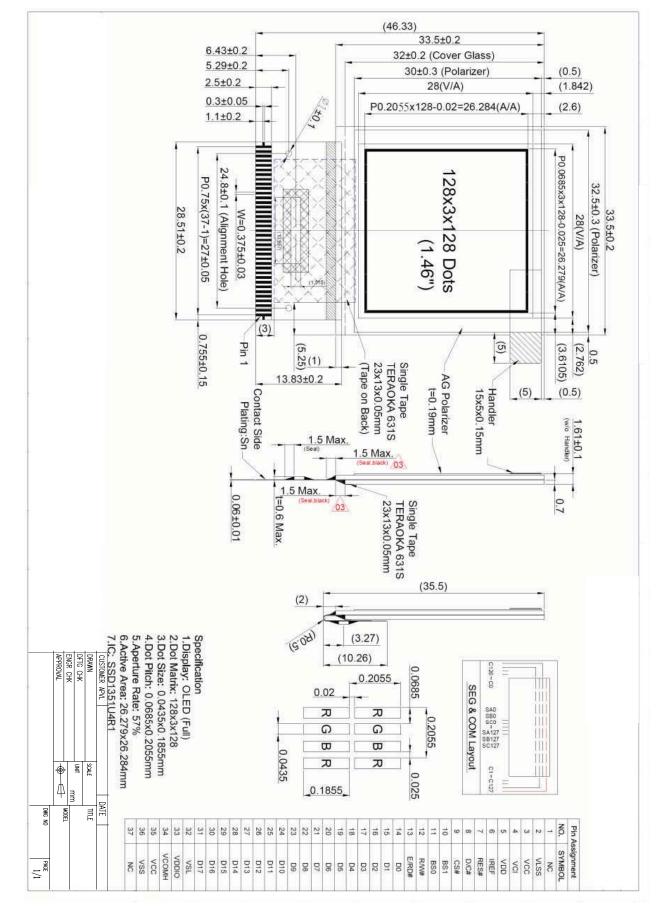


■ PHYSICAL DATA

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EXTERNAL DIMENSIONS





Items	Symbol	Min	Тур.	Max	Unit	Notes
	V _{CI}	-0.3	-	4	V	-
Supply voltage	V _{CC}	10	-	19	V	-
	V _{DDIO}	-0.5	-	V _{CI}	V	-
Operating temperature	Тор	-40	-	70	°C	-
Storage temperature	T _{ST}	-40	-	85	°C	-
Life time(90cd/m ²)	-	11,000	-	-	hour	1
Life time(70cd/m ²)	-	14,000	-	-	hour	2
Humidity	-	-	-	85	%RH	-

■ ABSOLUTE MAXIMUM RATINGS

Note:

(A) Under Vcc = 16.5V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m^2 :

- Master contrast setting : 0x0B
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 70 cd/m^2 :

- Master contrast setting : 0x09
- Red contrast setting : 0x66
- Green contrast setting : 0x6A
- Blue contrast setting : 0x89
- Frame rate : 105Hz
- Duty setting : 1/128



ELECTRICAL CHARACTERISTICS

•DC Characteristics

Items	Symbol	Conditions	Min	Тур.	Max	Unit
Analog power supply	V _{CC}		16	16.5	17	V
Digital power supply	V _{CI}		2.4	2.8	3.5	V
I/O voltage power supply	V _{DDIO}		1.65	-	V _{CI}	V
High level input	V _{IH}	$I_{OUT} = 100 \mu A, 3.3 MH$	0.8 x V _{DDIO}	-	V _{DDIO}	V
Low level input	V _{IL}	$I_{OUT} = 100 \mu A, 3.3 MH$	0	-	0.2xV _{DDIO}	V
High level output	Vон	$I_{OUT} = 100 \mu A, 3.3 MH$	0.9xV _{DDIO}	-	V _{DDIO}	V
Low level output	Vol	$I_{OUT} = 100 \mu A, 3.3 MH$	0	-	0.1xV _{DDIO}	V
Operating current for V _{DD}	I _{DD}		-	170	190	uA
		External VDD=2.6V	-	0.5	10	uA
Operating current for V _{DDIO}	I DDIO	Internal VDD	-	0.5	10	uA
		External VDD=2.6V	-	60	70	uA
Operating current for V _{CI}	I _{CI}	Internal VDD	-	255	280	uA
		External VDD=2.6V	-	1.15	1.26	mA
Operating current for V _{CC}	I _{CC}	Internal VDD	-	1.15	1.26	mA
		Contrast=FF	-	200	-	uA
Segment output current setting	I SEG	Contrast=7F	-	100	-	uA
		Contrast=3F	-	50	-	uA

ASI-O-146GAFFF80/M



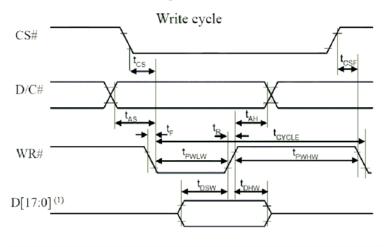
AC Characteristics

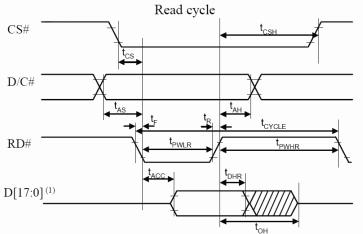
1. 80XX-Series MPU Parallel Interface Timing Characteristics:

8080-Series MCU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{CYCLE}	Clock Cycle Time	300	-		ns
t _{AS}	Address Setup Time	10	-	-	ns
t _{AH}	Address Hold Time	0	-		ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	7	-		ns
t _{DHR}	Read Data Hold Time	20		-	ns
t _{OH}	Output Disable Time	-		70	ns
t _{ACC}	Access Time		-	140	ns
tPWLR	Read Low Time	150	-	-	ns
tpwLW	Write Low Time	60	-		ns
t _{PWHR}	Read High Time	60	-	-	ns
tpwHW	Write High Time	60			ns
t _R	Rise Time	3 4 0	-	15	ns
t _F	Fall Time		-	15	ns
t _{cs}	Chip select setup time	0	-		ns
t _{CSH}	Chip select hold time to read signal	0	-	-	ns
t _{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics





Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.



2. Graphic Display Data Ram Address Map

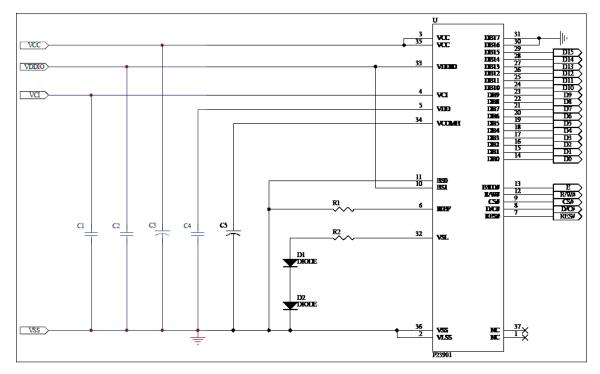
The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

					-									
Segment	Normal		0			1		2	 	126		127		
Address	Remapped		127			126		125	 	1		0		
Ce	olor	Α	В	С	Α	В	С	Α		C	A	В	C	
	Data	A5	B5	C5	A5	B5	C5	A5	 	C5	A5	B5	- C5	
F	Format	A4	B4	C4	A4	B4	C4	A4	 	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	 	C3	A3	B3	C3	
Common		A2	B2	C2	A2	B2	C2	A2	 	C2	A2	B2	C2	
Address		A1	B1	C1	A1	B1	C1	A1	 	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	 	C0	A0	B0	C0	Common
Normal	Remapped													output
0	127	6	6	6	6	6	6	6	 	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	 	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	 	6	6	6	6	COM2
3	124	б	Ý	б	б	б	б	б	 	б	б	б	б	COM3
4	123	6	6	6	6	6	6	6	 	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	 	6	6	6	6	COM5
6	121	6	6	no of bi	ts in this	cell	6	6	 	6	6	6	6	COM6
7	120								 	6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	 	:	:	:	:	:
:	:	:	:	:	:	:	:	:	 	:	:	:	:	:
:	:	:	:	:	:	:	:	:	 	:	:	:	:	:
123	4	6	6	6	6	6	6	6	 	6	6	6	6	:
124	3	6	6	6	6	6	6	6	 	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	 	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	 	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	 	6	6	6	6	COM127
SEG	output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	 	SC126	SA127	SB127	SC127	

262k Color Depth Graphic Display Data RAM Structure



3. Application Circuit



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 16bits interface



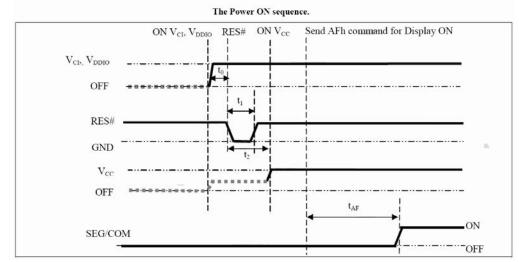
■ TIMING OF POWER SUPPLY

1.POWER ON/OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{Cl} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

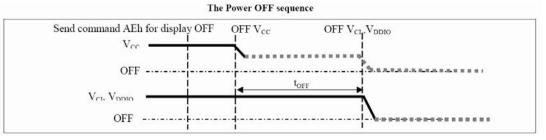
Power ON sequence:

- 1. Power ON V_{CI}, V_{DDIO}.
- 2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t₀) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us $(t_1)^{(4)}$ and then HIGH (logic high).
- 4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



Power OFF sequence:

- 1. Send command AEh for display OFF. 2. Power OFF $V_{CC}.^{(1),\,(2)}$
- 3. Wait for tOFF. Power OFF VCI, VDDIO. (where Minimum tOFF=80ms⁽³⁾, Typical $t_{OFF}=100$ ms)



Note:

- (1) Since an ESD protection circuit is connected between Vci, VDDIO and Vcc, Vcc becomes lower than Vciwhenever Vci, Vodio is ON and Vcc is OFF as shown in the dotted line of Vcc in above figures.
- (2) Vcc should be kept float (disable) when it is OFF.
- (3) VCI, VDDIO should not be Power OFF before Vcc Power OFF.
- (4) The register values are reset after t1.
- (5) Power pins (VDD, VCC) can never be pulled to ground under any circumstance.





■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items	Symbol	Min.	Тур.	Max.	Unit	Remark		
Normal mode lun	ninance	L	70	90	-	cd /m ²	Display average	
Standby mode lur	ninance	L	_	20	-	cd /m ²		
Response tir	ne	-	-	10	-	μs		
Normal mode c	current	-	-	30	32	mA	1	
Standby mode c	urrent	-	-	3	4	mA	2	
Normal mode power c	onsumption	-	-	495	528	mW	1	
Standby mode power of	consumption	-	-	49.5	66	mW	2	
	White	CIE x	0.24	0.28	0.32			
		CIE y	0.28	0.32	0.36			
	Red	CIE x	0.62	0.66	0.70			
Color Coordinate	Keu	CIE y	0.29	0.33	0.37	CIE1931	Darkroom	
	Crear	CIE x	0.26	0.30	0.34	CIEI931	Darktoom	
	Green	CIE y	0.59	0.63	0.67	-		
	Dlass	CIE x	0.10	0.14	0.18			
	Blue	CIE y	0.14	0.18	0.22			
Contrast Ra	tio*	Cr	20000:1	-	-		Darkroom	
Viewing Angle U	niformity	θ	160	-	-	Degree	-	

(1) Normal mode condition :

- Driving Voltage : 16.5V
- Master contrast setting : 0x0B
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

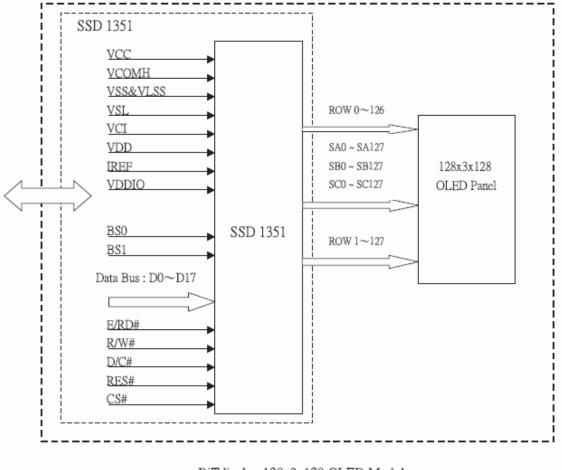
(2) Standby mode condition :

- Driving Voltage : 16.5V
- Master contrast setting : 0x04
- Red contrast setting : 0x4E
- Green contrast setting : 0x53
- Blue contrast setting : 0X6E
- Frame rate : 105Hz
- Duty setting : 1/128



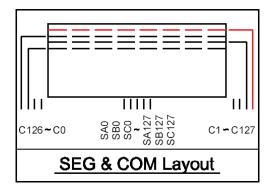
■ INTERFACE PIN CONNECTIONS

1.FUNCTION BLOCK DIAGRAM



RiTdisplay 128x3x128 OLED Module

2.PANEL LAYOUT DIAGRAM





3.PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VLSS	2	Analog system ground pin
VCC	3	Power supply for panel driving voltage.
VCI	4	Digital voltage power supply.
VDD	5	Power supply pin for core logic operation.
IREF	6	A resistor should be connected between this pin and VSS.
RES#	7	Hardware Reset pin (Low active).
D/C#	8	H: Data, L: Command.
CS#	9	Chip select pin.
BS1	10	Interface select pin.
BS0	11	Interface select pin.
R/W#	12	8080: data write enable pin; 6800:Read/Write select pin.
E/RD#	13	8080: data read enable pin; 6800:Read/Write enable pin.
D0	14	
D1	15	
D2	16	
D3	17	
D4	18	
D5	19	
D6	20	
D7	21	
D8	22	These pins are bi-directional data bus connecting to the
D9	23	MCU data bus.
D10	24	
D11	25	
D12	26	
D13	27	
D14	28	
D15	29	_
D16	30	
D17	31	
VSL	32	This is segment voltage reference pin.
VDDIO	33	Power supply for interface logic level.
VCOMH	34	COM signal deselected voltage level. A capacitor should be connected between this pin an VSS.
VCC	35	Power supply for panel driving voltage.
VSS	36	Ground.
NC	37	No connection.



RELIABILITY TESTS

	Item	Condition	Criterion		
High Te	emperature Storage (HTS)	85±2°C, 240 hours	 After testing, the function test is ok. After testing, no addition to the defect. 		
High Ter	nperature Operating (HTO)	$70\pm2^{\circ}$ C, 120 hours	3. After testing, the change of luminance should be within +/- 50% of initial value.		
Low Te	emperature Storage (LTS)	-40 $\pm 2^{\circ}$ C, 240 hours	 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 		
Low Ter	nperature Operating (LTO)	-40 $\pm 2^{\circ}$ C, 120 hours	0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on		
High Tempe	erature / High Humidity Storage (HTHHS)	65±3℃, 90%±3%RH, 96 hours	 1931 CIE coordinates. 5. After testing, the change of total current consumption should be 		
Thermal Shock (Non-operation) (TS)		-40±2°C ~ 25°C ~ 85±2°C (30min) (5min) (30min) 20cycles	within +/- 50% of initial value.		
Vibration (Packing) 10~55~10Hz,amplitu de 1.5mm, 1 hour for each direction x, y, z		1. One box for each test.			
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle	2. No addition to the cosmetic	and the electrical defects.		

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.

2) The HTHHS test is requested the Pure Water(Resistance > $10M\Omega$).





OUTGOING QUALITY CONTROL SPECIFICATION Standard

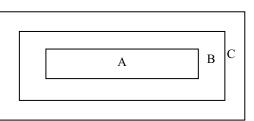
According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

Definition

1 Major defect : The defect that greatly affect the usability of product.

2 Minor defect : The other defects, such as cosmetic defects, etc.

3 Definition of inspection zone:



Zone A: Active Area

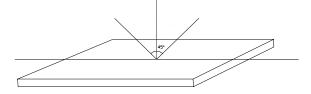
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

♦ Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5 ℃.



2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25 ± 5 °C.

♦Inspection Criteria

1 Major defect : AQL = 0.65

Item	Criterion				
	1. No display or abnormal display is not accepted				
Function Defect	2. Open or short is not accepted.				
	3. Power consumption exceeding the spec is not accepted.				
Outline Dimension	Outline dimension exceeding the spec is not accepted.				
Glass Crack	Glass crack tends to enlarge is not accepted.				

2 Minor Defect : AQL= 1.5



Item	Criterion								
	Size	(mm)	Accepted Q	ty					
Spot			Area A + Area B	Area C					
Defect (dimming		$\Phi \leq 0.10$	Ignored	1					
and		$0.10 < \Phi \le 0.15$	3						
lighting	X	0.15<Φ≦0. 20	1	Ignored					
spot)	¦ ≖ ´` ►I	0.20<Φ	0						
	Note : $\Phi = (x + y) /$	2							
Line	L (Length):mm	W (Width):mm	Area A + Area B	Area C					
Defect	/	W≦0.03	Ignored						
(dimming and	L≦3.0	$0.03 \le W \le 0.05$	2						
lighting	L≦2.0	$0.05 \le W \le 0.08$	1	Ignored					
line)	/	0.08 <w< td=""><td>As spot defect</td><td></td></w<>	As spot defect						
Remarks: Tl	ne total of spot defect	and line defect shall	not exceed 4 pcs.						
Polarizer	Stain which can be w	viped off lightly with	a soft cloth or simil	ar					
Stain	cleaning is accepted. Line Defect.	, otherwise, according	g to the Spot Defect	and the					
	1. If scratch can be seen during operation, according to the criterions								
	of the Spot Defect and the Line Defect.								
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :								
Polarizer	L (Length): mm	W (Width): mm	Area A + Area B	Area C					
Scratch	/	W≦0.03	Ignore						
	5.0 <l≦10.0< td=""><td>$0.03 \le W \le 0.05$</td><td>2</td><td></td></l≦10.0<>	$0.03 \le W \le 0.05$	2						
	L≦5.0	$0.05 \le W \le 0.08$	1	Ignore					
	/	0.08 <w< td=""><td>0</td><td></td></w<>	0						
	Si	ze	Area A + Area B	Area C					
		$\Phi \leq 0.20$	Ignored						
Polarizer Air Bubble		$0.20 < \Phi \le 0.50$	2						
	X	$0.50 < \Phi \le 0.80$	1	Ignored					
		$0.80{<}\Phi$	0						



	1. On the company		
Glass Defect (Glass Chiped)	1. On the corner	(mm)	
		X	≤ 2.0
		у	\leq S
		Z	≤ t
	z		
	2. On the bonding edge		
		(mm)	
	12	X	\leq a / 2
		У	\leq s / 3
		Z	\leq t
	the trans		
	3. On the other edges		
	Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z	(mm) X y z	$\frac{\leq a / 5}{\leq 1.0}$ $\leq t$
	Note: t: glass thickness ; s: pad width ; a: the length of the edge		
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted		
Pixel Size	The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec		
Luminance	Refer to the spec or the reference sample		
Color	Refer to the spec or the reference sample		



■ CAUTIONS IN USING OLED MODULE

Precautions For Handling OLED Module:

- 1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
- 2. Do not attempt to disassemble or process the OLED Module.
- 3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
- 4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
- 5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
- 6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.

vi. Be sure to use anti-static package.

- 7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
- 8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
- 9. When the logic circuit power is off, do not apply the input signals.
- 10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
- 11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module' s life time, even make it damaged.
- 12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.



13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

Precautions For Soldering OLED Module:

- 1. Soldering temperature : $260^{\circ}C \pm 10^{\circ}C$.
- 2. Soldering time : 3-4 sec.
- 3. Repeating time : no more than 3 times.
- 4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

Precautions For Storing OLED Module:

- 1. Be sure to store the OLED Module in the vacuum bag with dessicant.
- 2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
- 3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
- 4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
- 5. It is recommended to keep the temperature between 0° C and 30° C, the relative humidity not over 60%.

♦ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

♦Return OLED Module Under Warranty:

- 1. No warranty in the case that the precautions are disregarded.
- 2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.