ALL SHORE INDUSTRIES

ASI-O-09112832ES-PT-EBS/M

No.	Items	Specification	Unit
1	Display Mode	Passive Matrix OLED	-
2	Display Color	Monochrome (Blue)	-
3	Duty	1/32	-
4	Resolution	128(H) x 32 (V)	Pixel
5	Active Area	22.375 (W) x 5.58 (H)	mm^2
6	Outline Dimension	26.90 (W) x 13.70 (H) x 1.28 (D)	mm^3
7	Dot Pitch	0.175 (W) x 0.175 (H)	mm^2
8	Dot Size	0.15 (W) x 0.155 (H)	mm^2
9	Aperture Rate	76	%
10	Driver IC	SHM6211	-
11	Interface	8-bit 8080,8-bit 6800,I2C,Serial interface	-
12	Weight	0.96 ± 10%	g

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2013-06-06	Initial Release	

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■ PHYSICAL DATA

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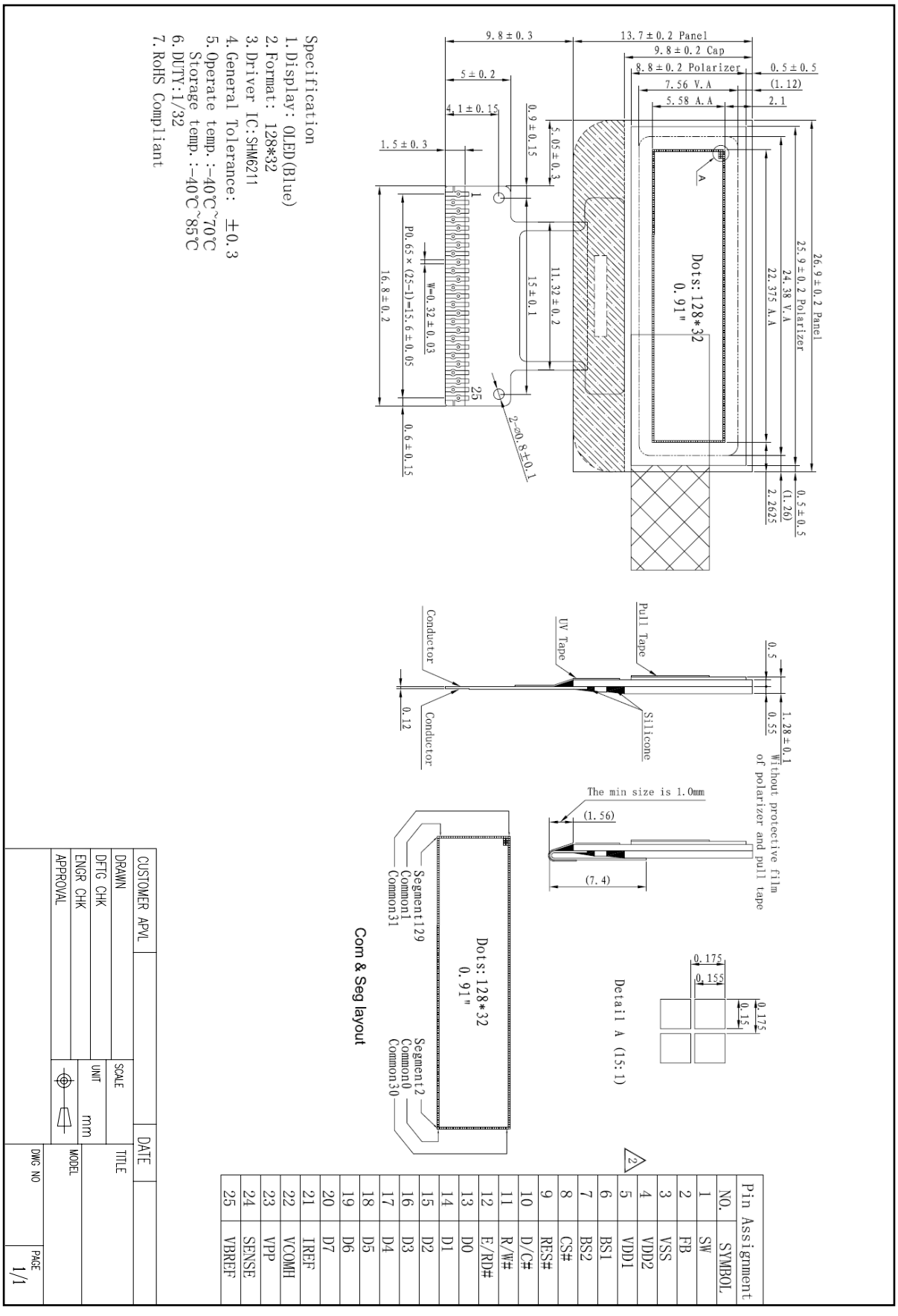
■ EXTERNAL DIMENSIONS



■ ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
DC Supply Voltage	VDD1	-0.3	+3.6	V	IC maximum rating
	VDD2	-0.3	+3.6	V	IC maximum rating
OLED Operating voltage	VPP	0	+13	V	IC maximum rating
Operating Temp.	Top	-40	+70	℃	-
Storage Temp	Tstg	-40	+85	℃	-
Operation life time(80cd/m^2)	-	10,000	-	Hrs	-

Note 1: All the above voltages are on the basis of "V_{SS} 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.Also,for normal operations,it is desirable to use this module under the conditions according to electro-optical characteristics .If this module is used beyond these conditions,malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: V_{PP} 8.0V, T_a 25℃, 50% Checkerboard.
Software configuration follows Actual Application Example .
End of lifetime is specified as 50% of initial brightness reached.The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD1	22±3°C, 55±15%R.H	1.65	3.0	3.5	V
	VDD2	22±3°C, 55±15%R.H	2.4	3.3	3.5	V
OLED Driver Supply Voltage	VPP	22±3°C, 55±15%R.H	7.5	8.0	8.5	V
High-level Input Voltage	V_{IH}	-	0.8×VDD1	-	VDD1	V
Low-level Input Voltage	V_{IL}	-	VSS	-	0.2×VDD1	V
High-level Output Voltage	V_{OH}	-	0.8×VDD1	-	VDD1	V
Low-level Output Voltage	V_{OL}	-	VSS	-	0.2×VDD1	V

Note : The VPP input must be kept in a stable value; ripple and noise are not allowed.

◆AC Characteristics

1. 8080-Series MPU Parallel Interface Timing Characteristics

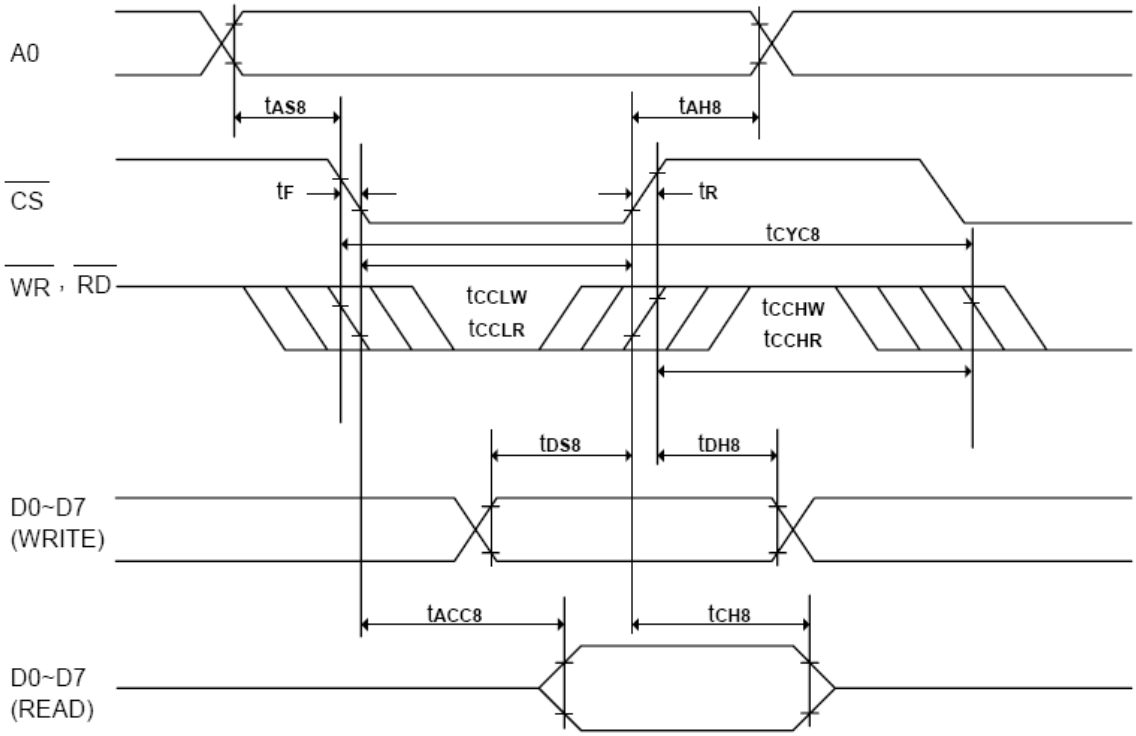
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	200	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	240	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	200	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

8080-series parallel interface characteristics



2. 6800-Series MPU Parallel Interface Timing Characteristics

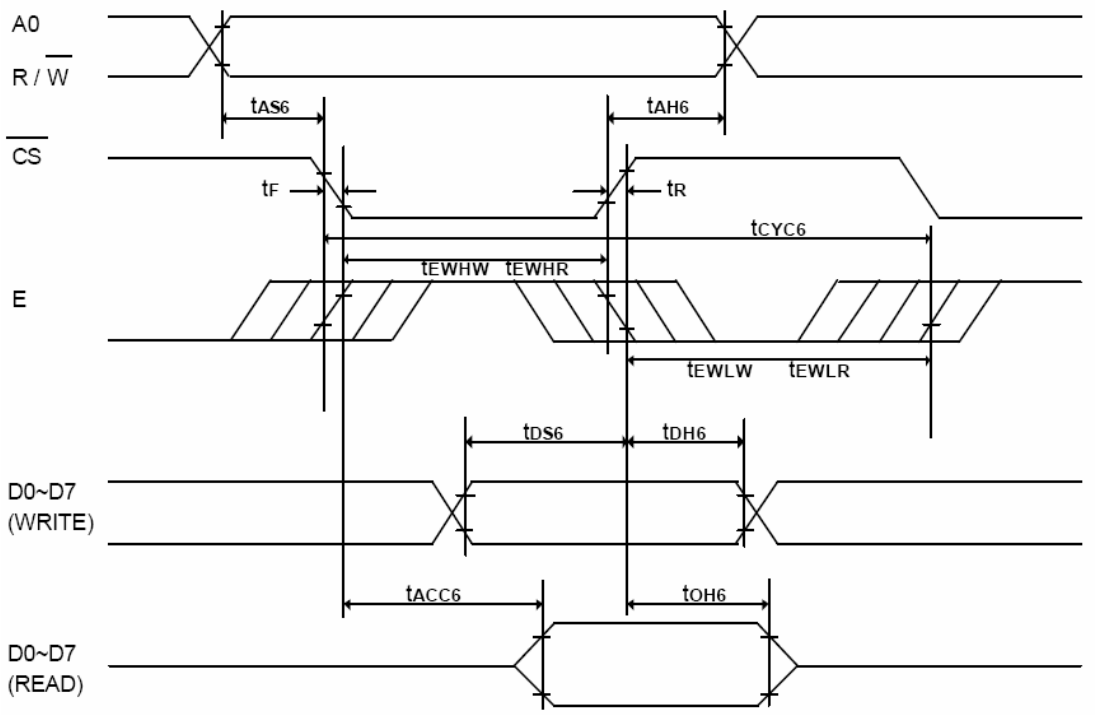
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

6800-series parallel interface characteristics



3. Serial Interface Timing Characteristics

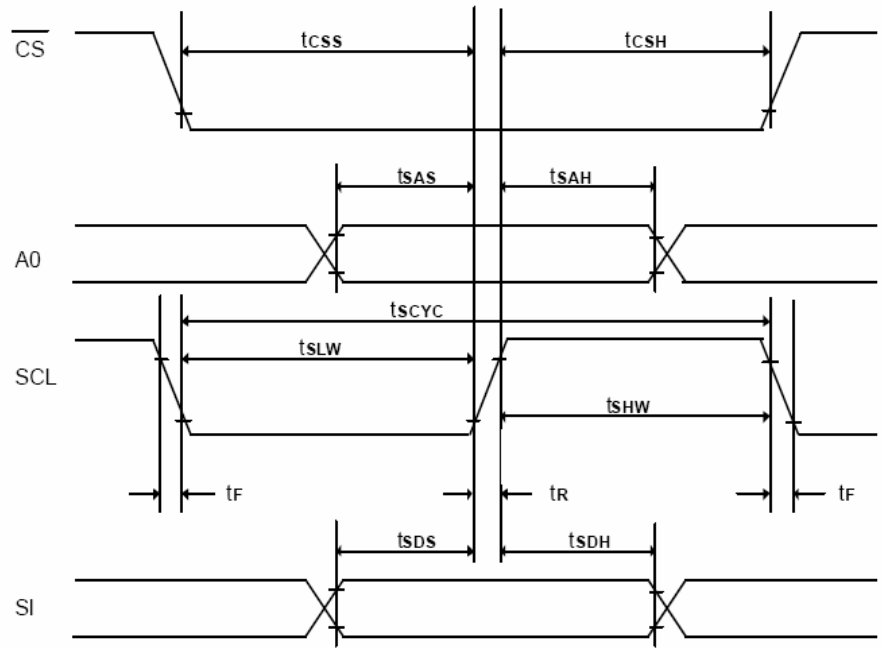
(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(VDD1 = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	

Serial Interface characteristics

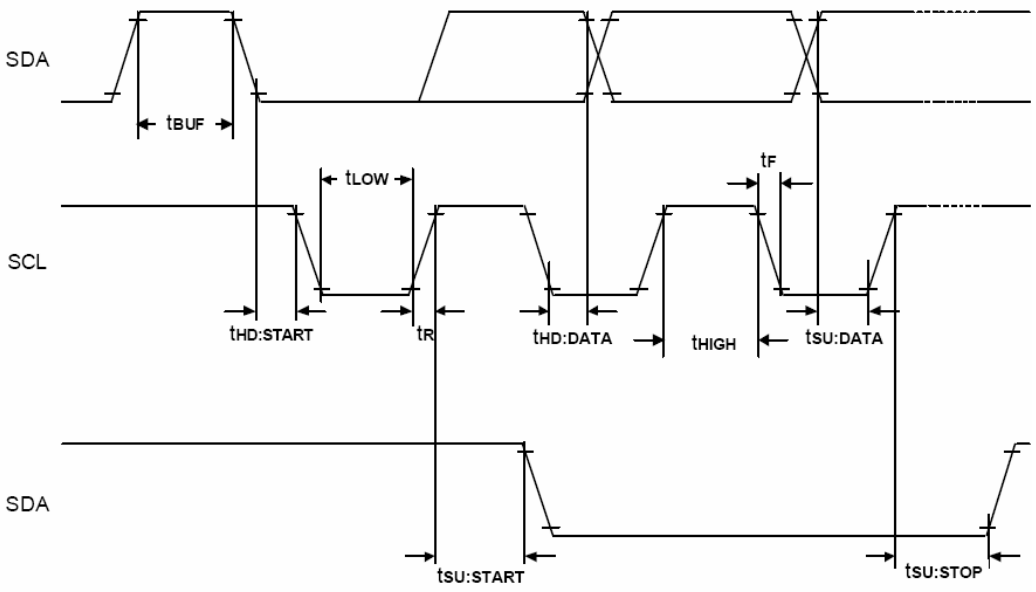


4.I² C Interface Timing Characteristics

(VDD1 = 1.65V to 3.5V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	uS	
THIGH	SCL clock H pulse width	0.6	-	-	uS	
TSU:DATA	data setup time	100	-	-	nS	
THD:DATA	data hold time	0	-	0.9	uS	
TR	SCL，SDA rise time	20+0.1Cb	-	300	nS	
TF	SCL，SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup time for re-START	0.6	-	-	uS	
THD:START	START Hold time	0.6	-	-	uS	
TSU:STOP	Setup time for STOP	0.6	-	-	uS	
TBUF	Bus free times between STOP and START condition	1.3	-	-	uS	

Serial Interface characteristics

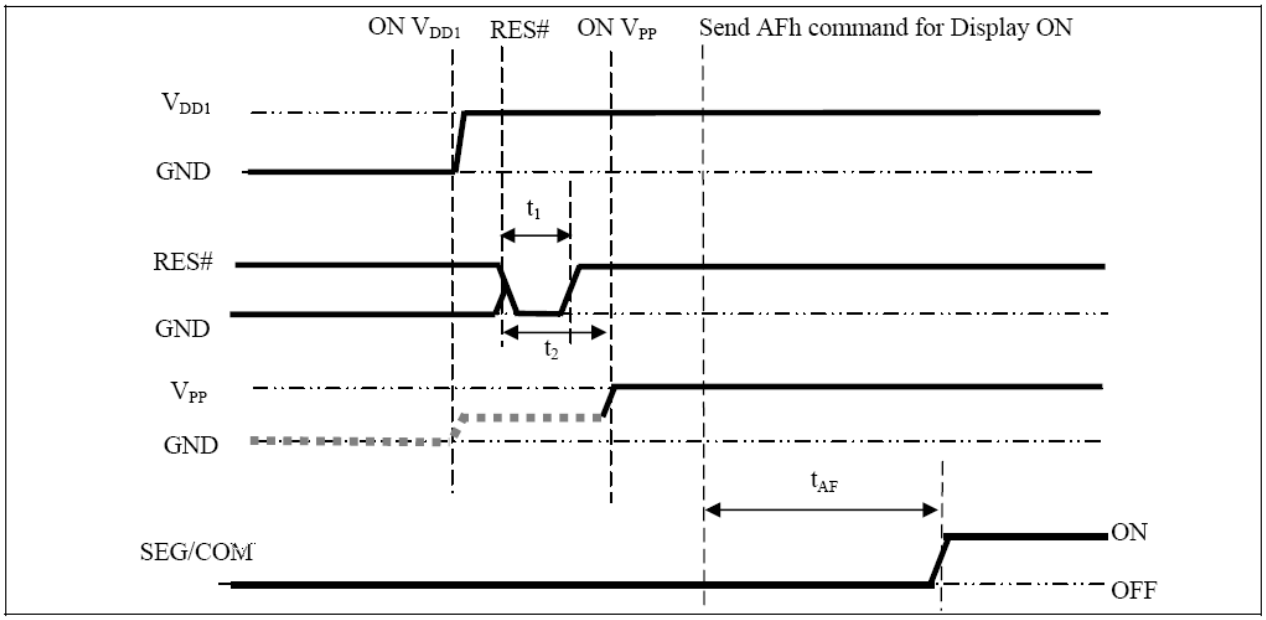


■ TIMING OF POWER SUPPLY

1 Power ON and Power OFF Sequence

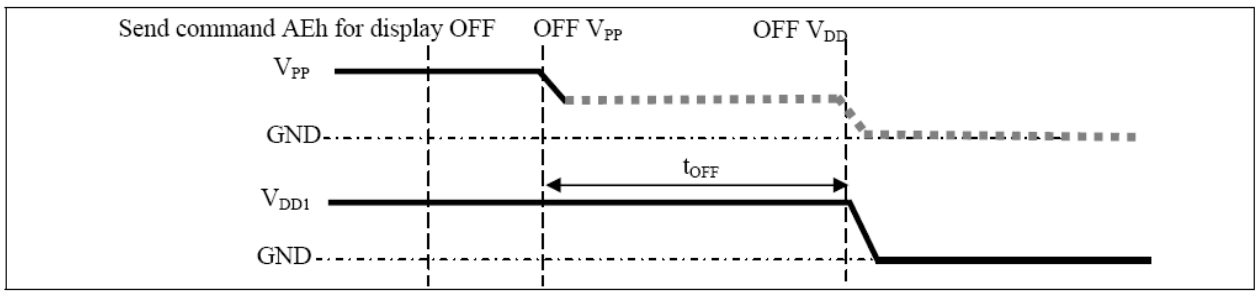
Power ON Sequence:

1. Power ON VDD1.
2. After VDD1 become stable, set RES pin LOW (logic low) for at least 5us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 5us (t_2). Then Power ON VPP. (1)
4. After V_{PP} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF Sequence:

1. Send command AEh for display OFF.
2. Power OFF VPP.(1), (2)
3. Wait for t_{OFF}. Power OFF VDD1. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VDD1 and VPP, VPP becomes lower than VDD1 whenever VDD1 is ON and VPP is OFF as shown in the dotted line of VPP in above figures.

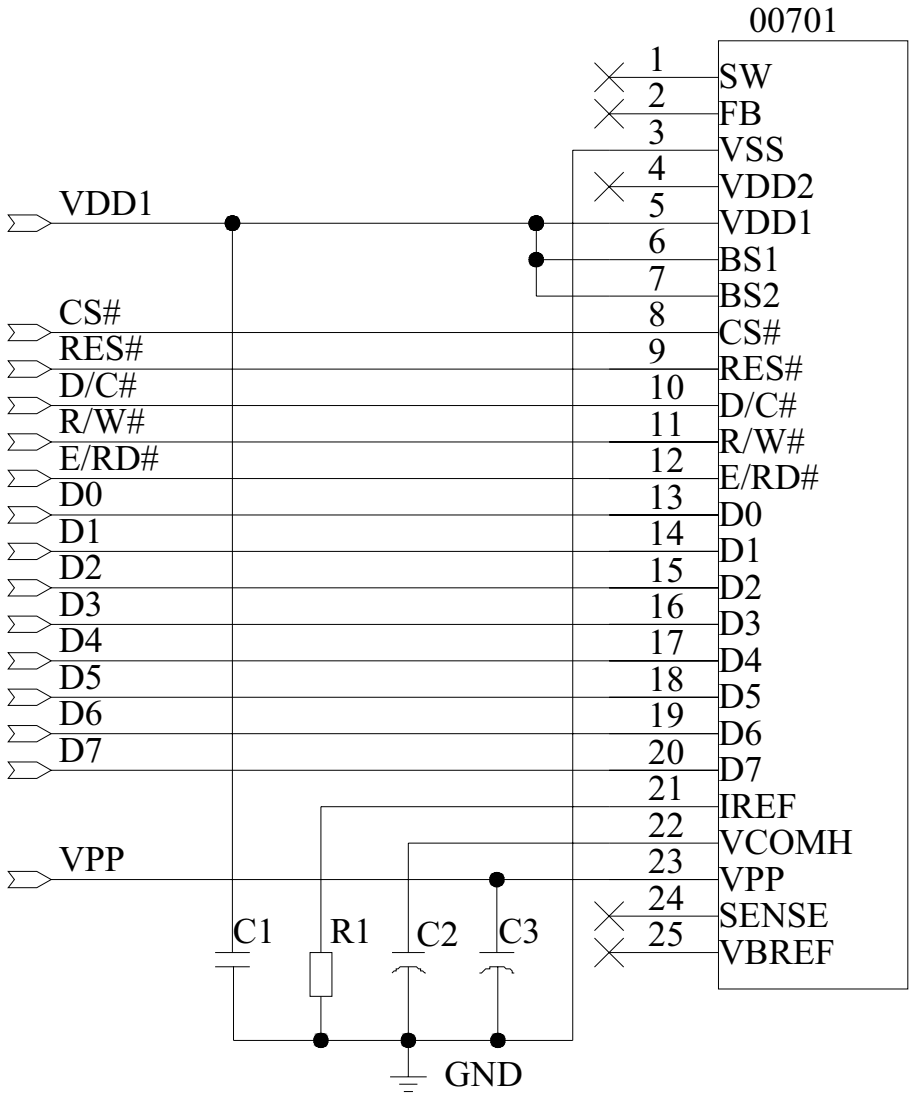
(2). VPP should be kept float (disable) when it is OFF.

2 Application Circuit

2.1 Under external VCC Mode,the charge Pump Setting (ADh) must be set as follow:

ADh:DC-DC Control Mode Set 8Ah:DC-DC is disable

(1).The configuration for 8080-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7], RD#, R/W#, D/C#, RES#, CS#

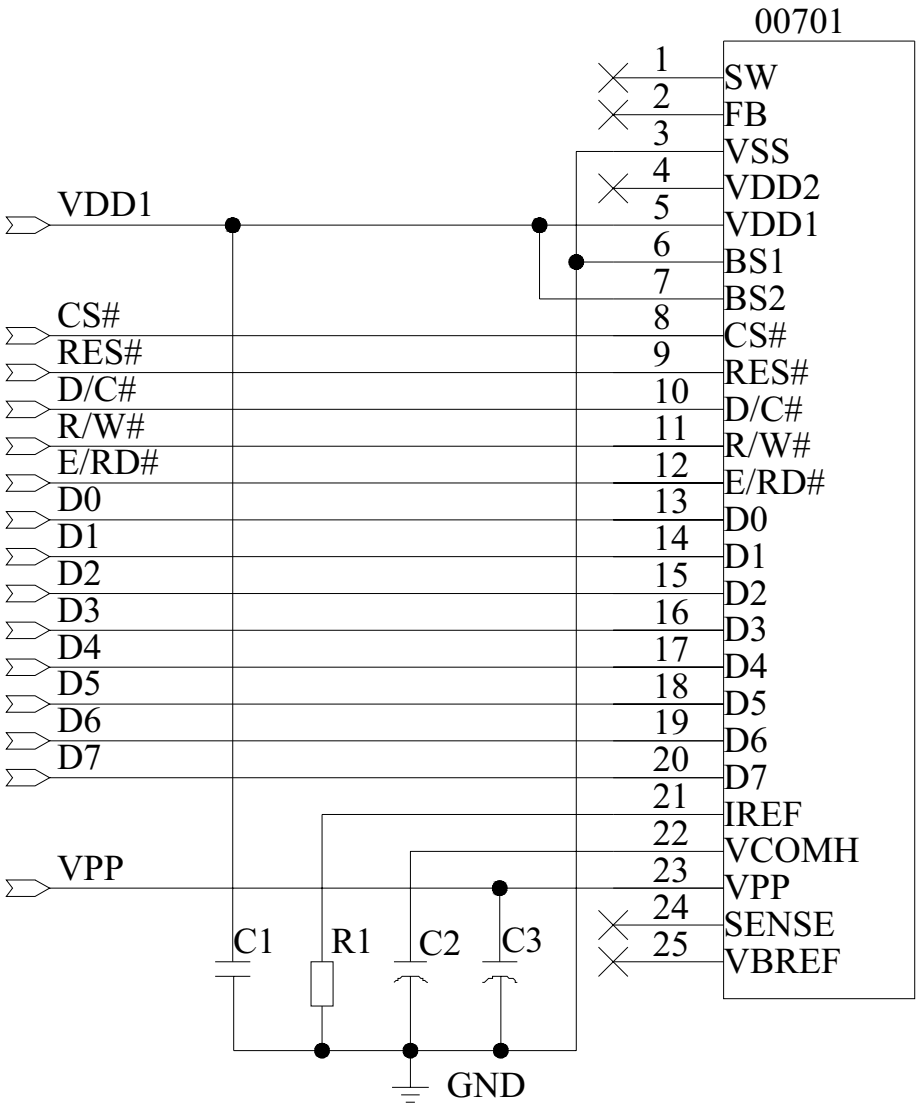
Recommended components

C1: 0.1uF-0603-X7R±10%.ROHS

C2,C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910Kohm.ROHS

(2).The configuration for 6800-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7], RD#, R/W#, D/C#, RES#, CS#

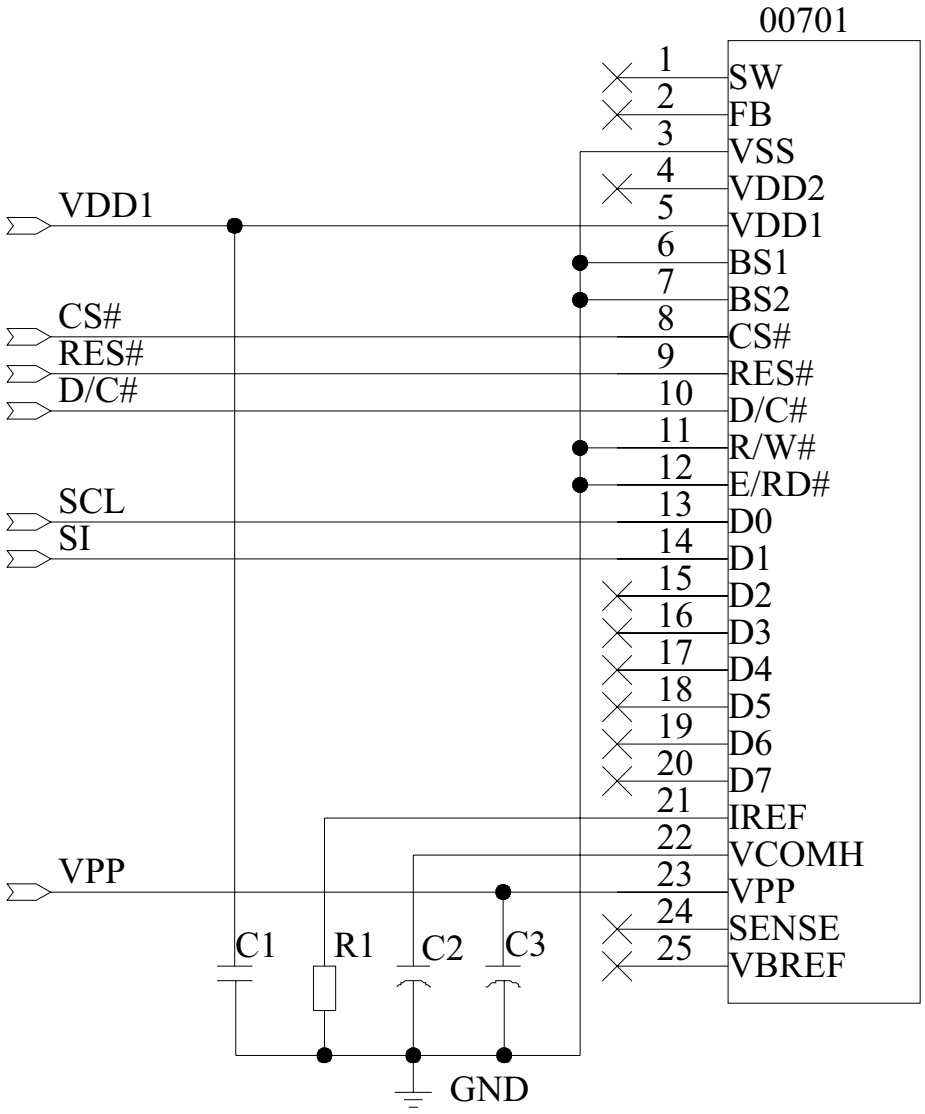
Recommended components

C1: 0.1uF-0603-X7R±10%.ROHS

C2,C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910Kohm.ROHS

(3).The configuration for SPI interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface:SCL,SI, D/C#, RES#, CS#

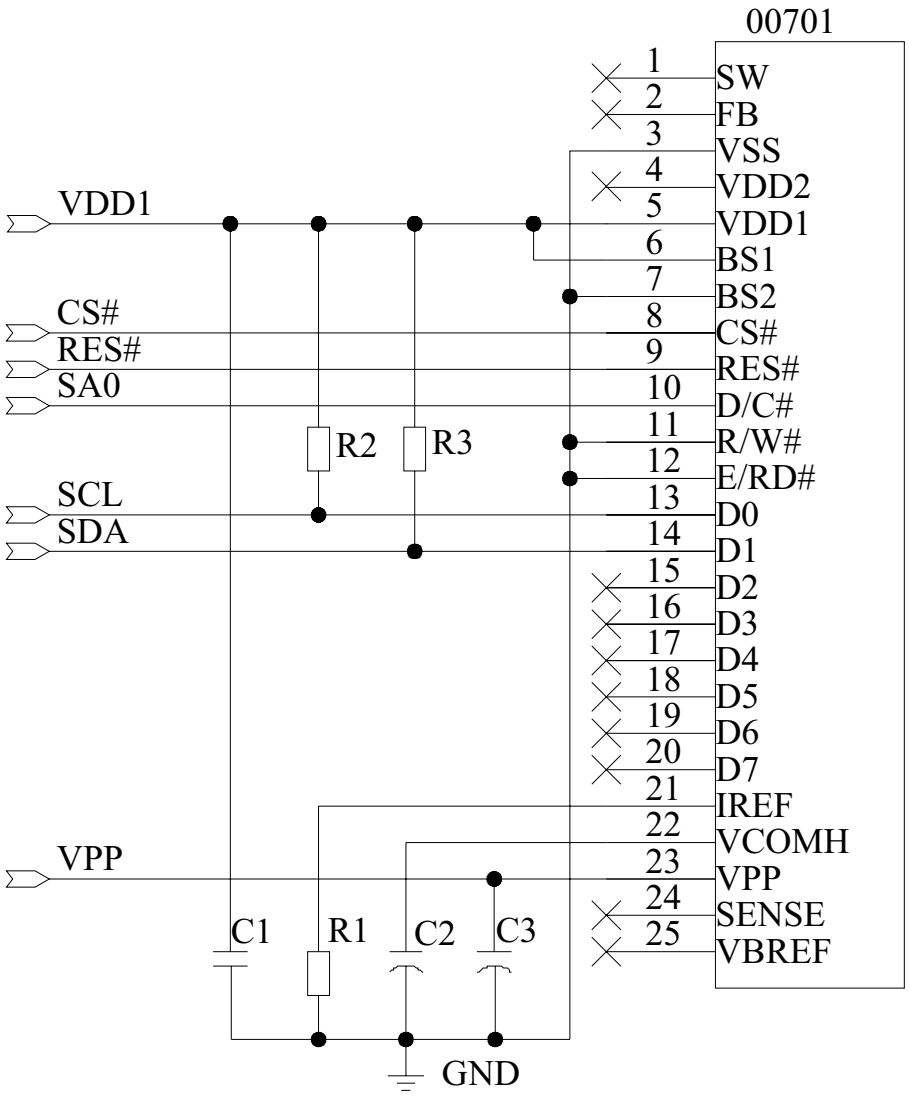
Recommended components

C1: 0.1uF-0603-X7R±10%.ROHS

C2,C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910Kohm.ROHS

(4).The configuration for I² C interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SDA,SA0, RES#, CS#

Recommended components

C1: 0.1uF-0603-X7R±10%.ROHS

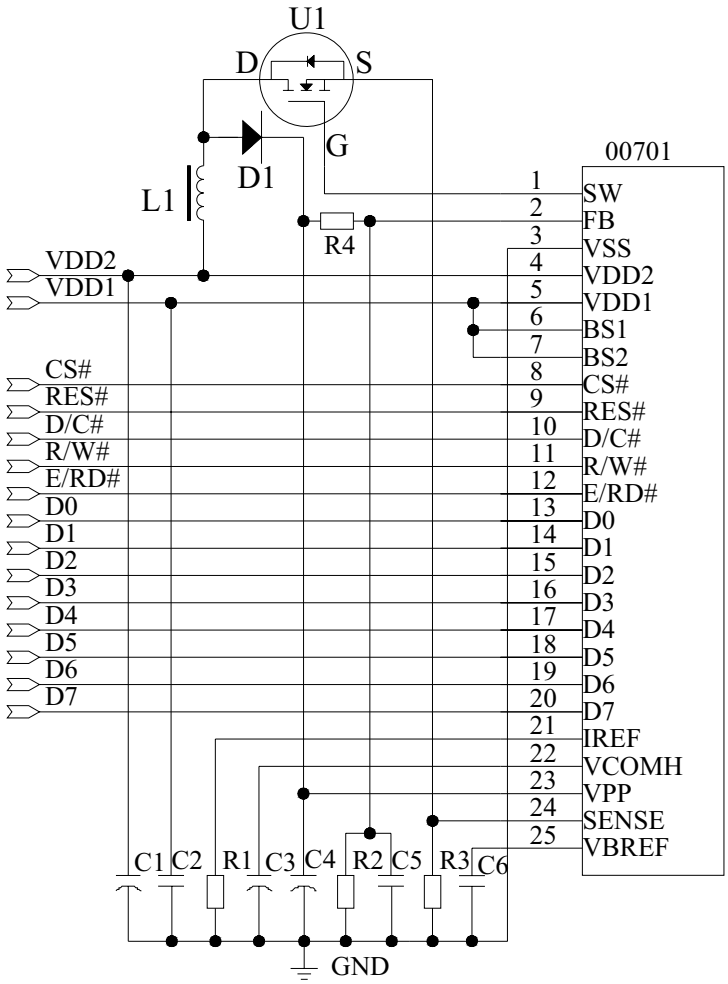
C2,C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 910Kohm.ROHS

R2,R3: 0603 1/10W +/-5% 10Kohm.ROHS

2.2 Under Internal DC/DC Mode,the charge Pump Setting (ADh) must be set as follow:

The configuration for 8080-parallel interface mode, Internal DC/DC Circuit is shown in the following Diagram:



Pin connected to MCU interface: D[7:0], RD, WR, A0, RES, A0

Recommended components

C1, C3,C4: 4.7μF/25V.ROHS (Tantalum Capacitors)

C2: 0.1uF-0603-X7R±10%.ROHS

C5: 1000pF-0603-X7R±10%.ROHS

C6: 1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 910Kohm.ROHS

R2: 0603 1/10W +/-1% 120Kohm.ROHS

R3: 0805 1/10W +/-1% 1/2W 0.12 ohm.ROHS

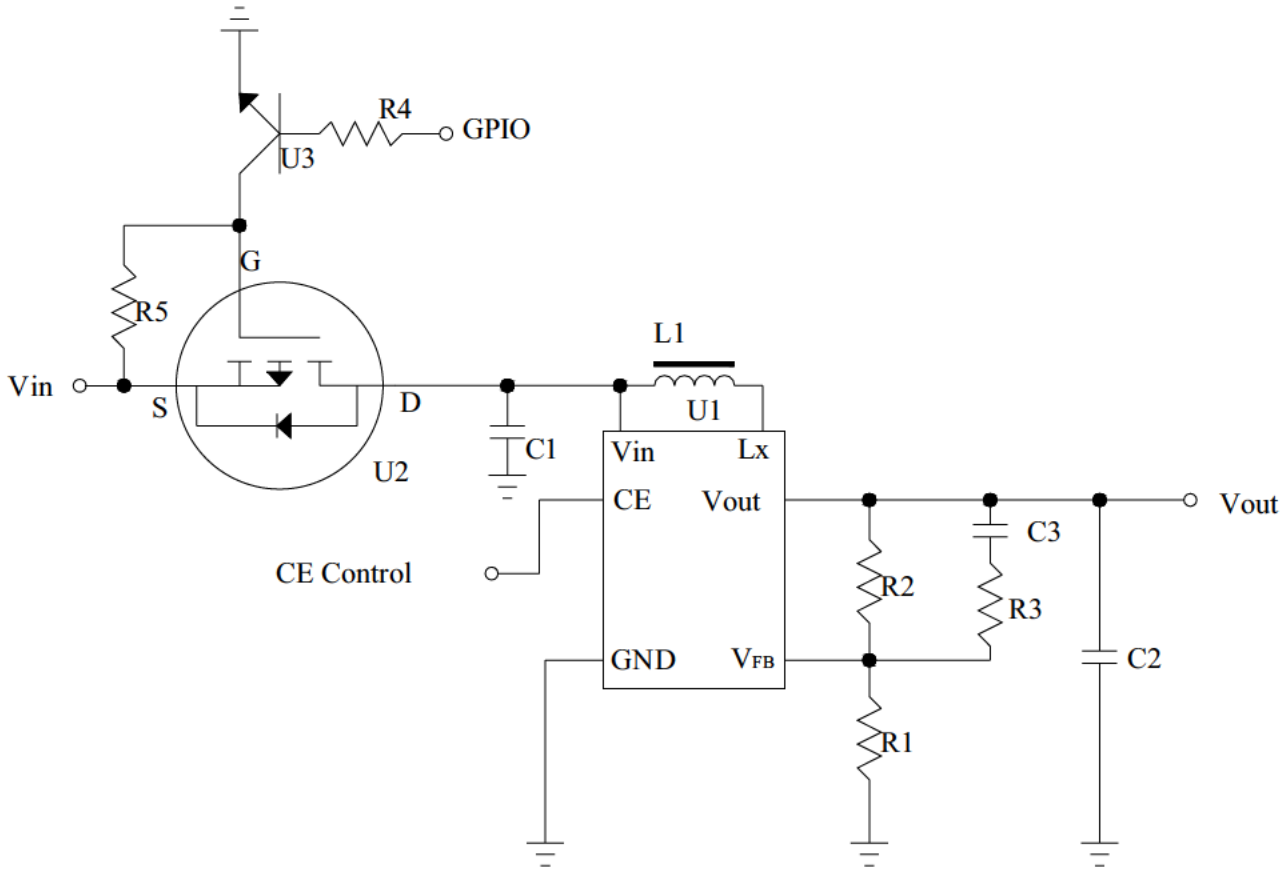
R4: 0603 1/10W +/-1% 620Kohm.ROHS

L1:LQH3C100K24

D1:20V@0.5A,MBR0520

U1:MGSF1N02LT1

3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-1% 10Kohm.ROHS
The R2	: 0603 1/10W +/-1% 70Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338N
The U3	: 8050

4 Display Control Instruction

Refer to SP5010 IC Specification.

5 Recommended Software Initialization

```
void init  program()
{
        write  c(0xae);          // display off
        write  c(0xd5);          //Set Display Clock Divide Ratio/Oscillator Frequency
        write  c(0x51);          //104HZ
        write  c(0xa8);          //Set Multiplex Ratio
        write  c(0x1f);          //set 32 mux
        write  c(0xd9);          //Set Pre-charge Period
        write  c(0x22);
        write  c(0xa1);          //seg re-map 127->0
        write  c(0xc8);          //COM scan direction COM(N-1)-->COM0
        write  c(0xda);          //Set COM Pins Hardware Configuration
        write  c(0x12);
        write  c(0x81);          //Set Contrast Control
        write  c(0x28);
        write  c(0xb0);          //Set Page Address
        write  c(0x10);          //Set Higher Column Address
        write  c(0x02);          //Set Lower Column Address
        write  c(0xd3);          //Set Display offset
        write  c(0x00);
        write  c(0x40);          //Set Display Start Line
        write  c(0xa6);          //Display Normal
        write  c(0xa4);          //Entire Display Off
        write  c(0xdb);          //Set VCOMH Level
        write  c(0x35);          //0.77*VCC
        write  c(0xaf);          //display on
}
```

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

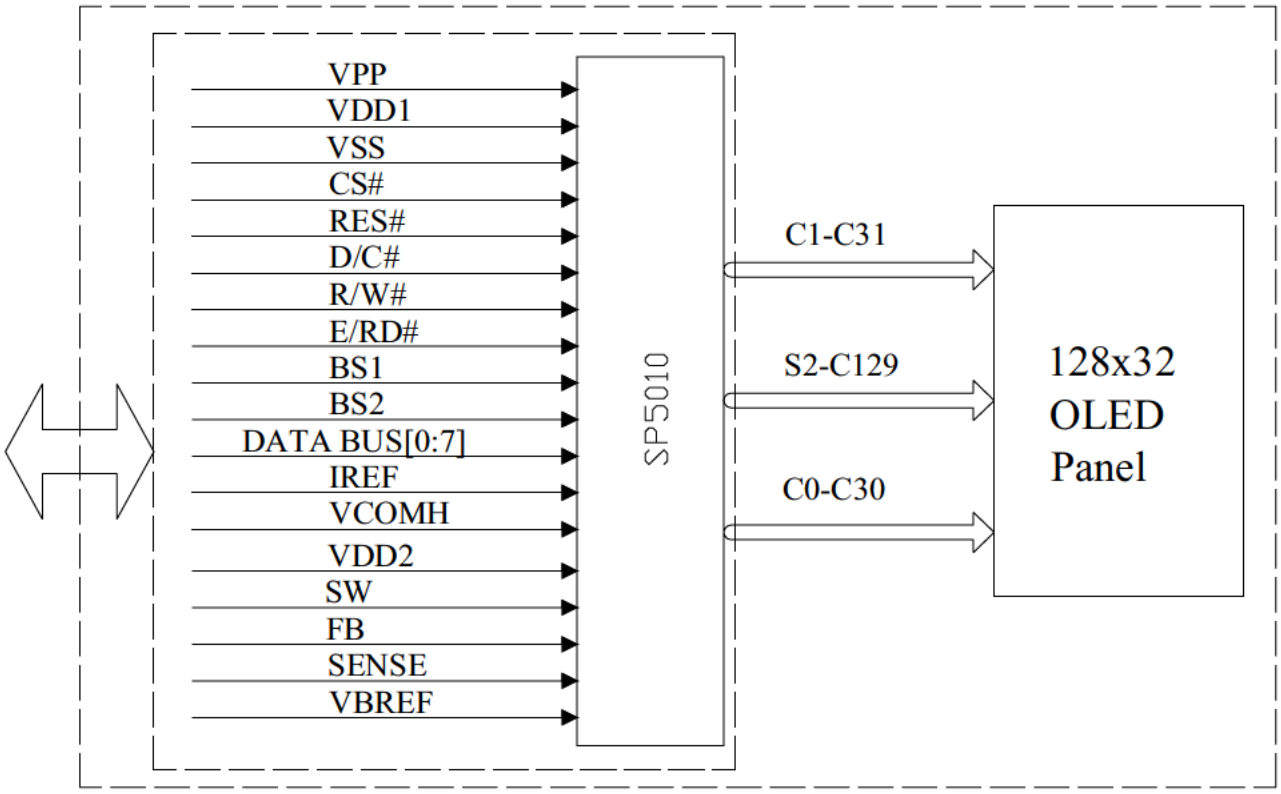
ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1)	60	80	-	cd/m^2
Sleep mode current consumption in VDD1&VDD2	ISP	During sleep,TA=+25℃, VDD1=3V,VDD2=3V	-	0.01	5	uA
Sleep mode current consumption in VPP		During sleep,TA=+25℃, VPP=9V	-	0.01	5	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)	-	40	55	mW
C.I.E(Blue)	(x)	x,y(CIE1931)	0.12	0.16	0.20	-
	(y)		0.23	0.27	0.31	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

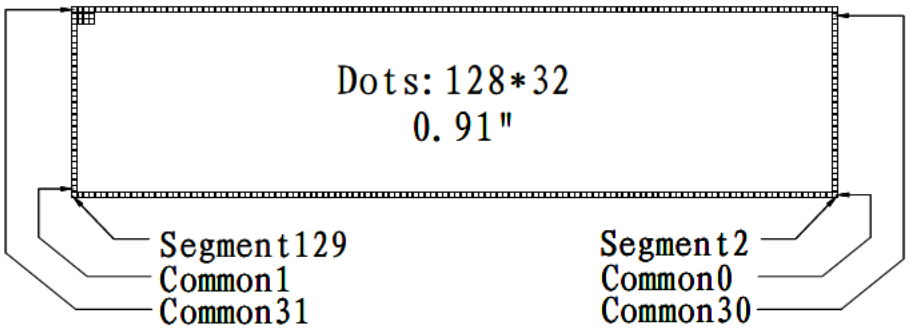
- Driving voltage : 8V
- Contrast setting : 0x28
- Frame rate : 104Hz
- Duty setting : 1/32

■ INTERFACE PIN CONNECTIONS

1 Function Block Diagram



2 Panel Layout Diagram



Com & Seg layout

3 Module Interface

<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>SW</td><td>This is an output pad driving the gate of the external NMOS of the booster circuit</td></tr>
<tr><td>2</td><td>FB</td><td>This is a feedback resistor input pad for the booster circuit.
It is used to adjust the booster output volatge level,VPP.</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>4</td><td>VDD2</td><td>2.4-3.5V power supply pad for the internal buffer of the DC-DC voltage converter</td></tr>
<tr><td>5</td><td>VDD1</td><td>Power supply output for pad option:1.65-3.5V</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2"><table>
<tr><td>Pin Name</td><td>6800-Parallel Interface</td><td>8080-Parallel Interface</td><td>SPI Interface</td><td>I² C Interface</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>This pad is the chip select input.When CS=“L”,then the chip select becomes active,
And data/command I/O is enabled.</td></tr>
<tr><td>9</td><td>RES#</td><td>This is a reset signal input pad.Then RES is set to “L”,the settings are initialized.
The reset operation is performed by the RES signal level.</td></tr>
<tr><td>10</td><td>D/C#</td><td>This is the data/command control pad that determines whether the data bits are data or a command.
A0=”H”:the inputs at D0 to D7 are treated as display data.
A0=”L”:the inputs at D0 to D7 are transferred to the command registers.
In I² C interface, this pad serves as SA0 to distinguish the different address of OLED driver</td></tr>
<tr><td>11</td><td>R/W#</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU,this is active LOW.This pad connects to the 8080 MPU WR signal.
The signals on the data bus are latched at the rising edge of the WR signal
Thwn connected to a 6800 Series MPU:This is the resd/write control signal input terminal
When WR=”H”:Read.
When WR=”L”:Write.</td></tr>
<tr><td>12</td><td>E/RD#</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU,it is active LOW.This pad is connected to the RD signal of the 8080 series MPU,and the SP5010 data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU,this is active HIGH.This is used as an enable clock
Input of 6800 series MPU.
When RD=”H”:Enable
When RD=”L”:Disable</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus
When the serial interface is selected,then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI).
Ath this time,D2 to D7 are set to high impedance.
When the I² C interface is selected,then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA).
At this time,D2to D7 are set to high impedance</td></tr>
<tr><td>21</td><td>IREF</td><td>This is a segment current reference pad.
A resistor should be connected between this pad and VSS.Set the current at 10uA</td></tr>
<tr><td>22</td><td>VCOMH</td><td>This is a pad for the voltage output high level for common signals.</td></tr>
<tr><td>23</td><td>VPP</td><td>This is the most positive voltage supply pad of the chip
It should be supplied externally</td></tr>
<tr><td>24</td><td>SENSE</td><td>This is a source current pad of the external NMOS of the booster circuit</td></tr>
<tr><td>25</td><td>VBREF</td><td>This is an internal voltage reference pad for booster circuit.
A stabilzation capacitor,typical 1uF,should be connected to VSS.</td></tr>
</table>

■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		85±2℃, 240 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 240 hours	
Low Temperature Storage (LTS)		-40±2℃, 240 hours	
Low Temperature Operating (LTO)		-40±2℃, 240 hours	
High Temperature / High Humidity Storage (HTHHS)		60±3℃, 90%±3%RH, 240 hours	
Thermal Shock (Non-operation) (TS)		-40±2℃ ~ 25℃ ~ 85±2℃ (30min) (5min) (30min) 30cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).

■OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

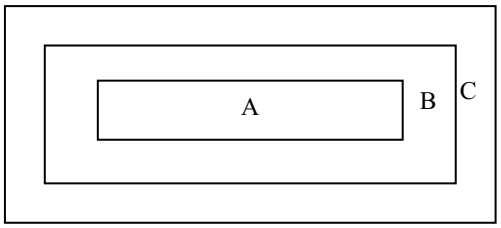
According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.

2 Minor defect : The other defects, such as cosmetic defects, etc.

3 Definition of inspection zone:



Zone A: Active Area

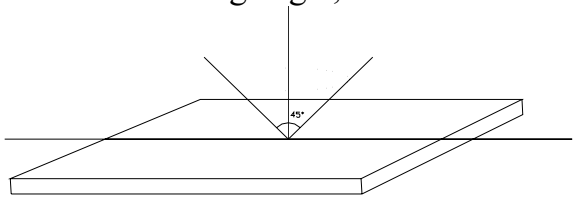
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



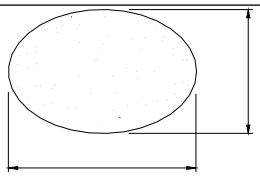
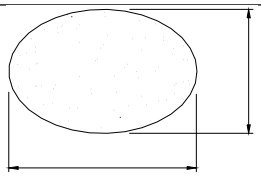
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

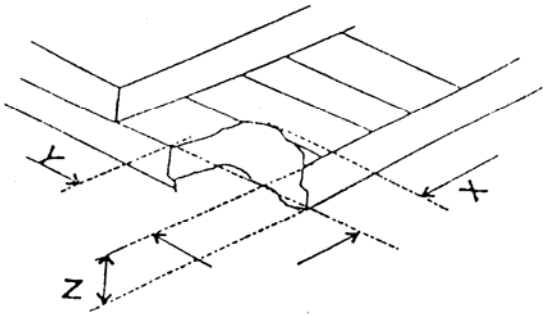
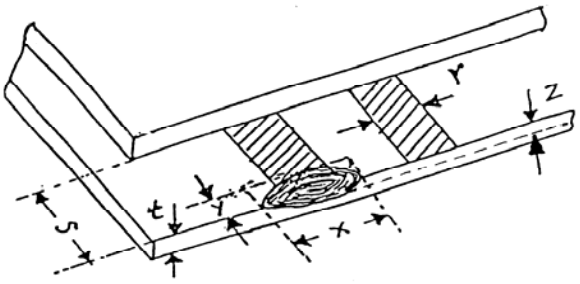
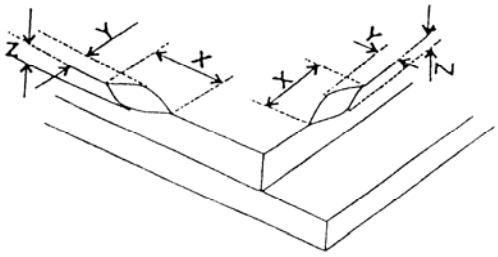
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="2">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td><td>0.20＜Φ</td><td>0</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="8">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0＜L≦10.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦5.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50＜Φ≦0.80</td><td>1</td></tr>
<tr><td>0.80＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 2.0</td></tr><tr><td>y</td><td>≤ S</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 2</td></tr><tr><td>y</td><td>≤ s / 3</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 5</td></tr><tr><td>y</td><td>≤ 1.0</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.