ALL SHORE INDUSTRIES

ASI-A-128648S-BN-EWD/U

Item	Contents	Unit
LCD type	STN NEGATIVE BLUE	-
Viewing direction	6:00	O'Clock
Module size (W×H×T)	65.20×32.90×5.35 (excluded FPC length)	mm
Viewing area (W×H)	60.00×21.70	mm
Driver IC	ST7567	-
Number of dots	128X64	-
Backlight type	3 LEDS White 3.0V 45mA	-
Interface type	Serial/parallel interface	-
Operating temperature	-20 ~ 70	ºC
Storage temperature	-30 ~ 80	ºC

REVISION HISTORY:				
Revision	Date	Description	Written By	Approved By
1.0	2022-08-29			

CONTENTS

1.0 GENERAL SPECIFICATION

Item	Contents	Unit
LCD type	STN NEGATIVE BLUE	-
Viewing direction	6:00	O'Clock
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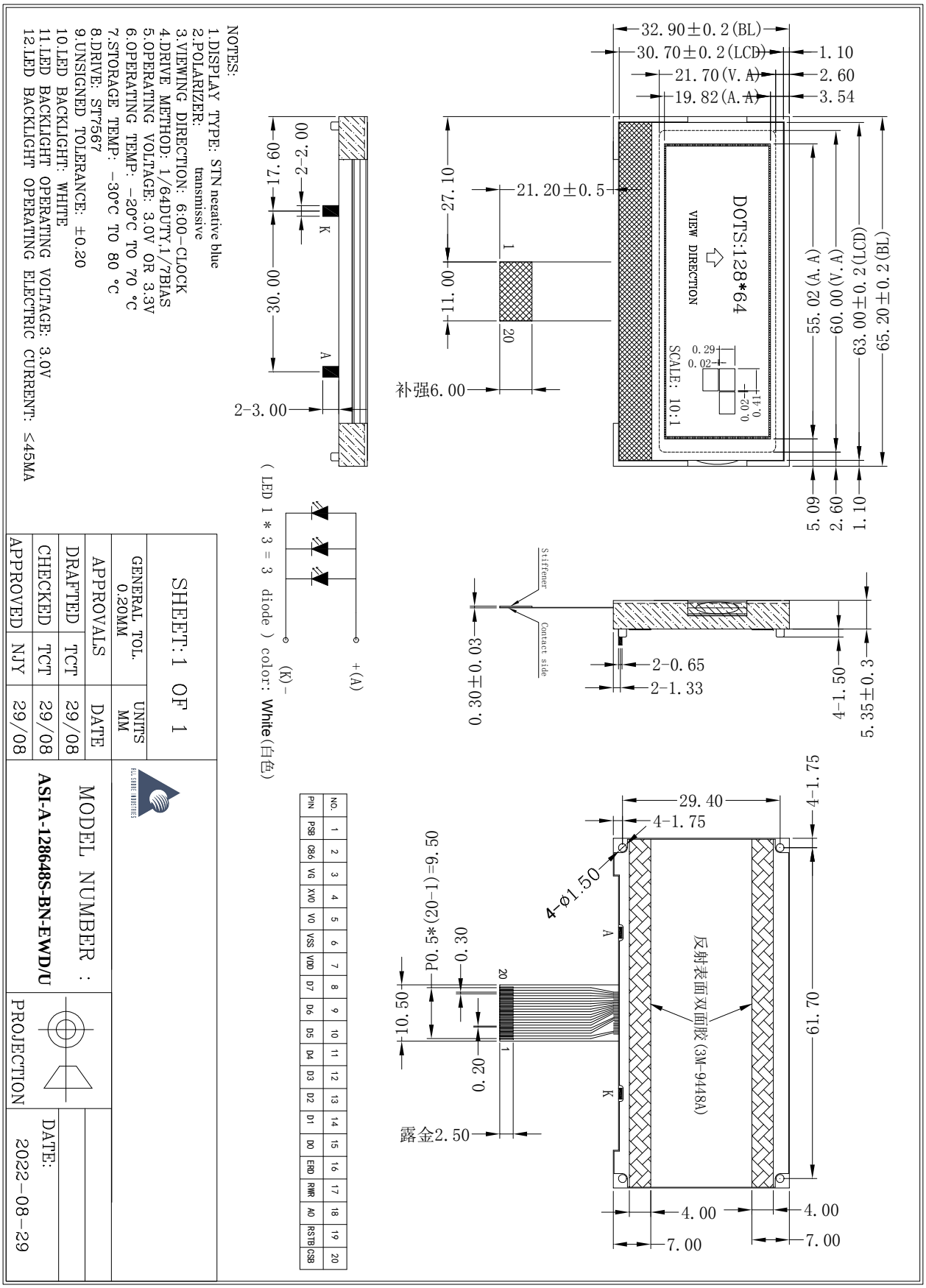
Number of dots	128X64	-
Backlight type	3 LEDS White 3.0V 45mA	-
Interface type	Serial/parallel interface	-
Operating temperature	-20 ~ 70	ºC
Storage temperature	-30 ~ 80	ºC

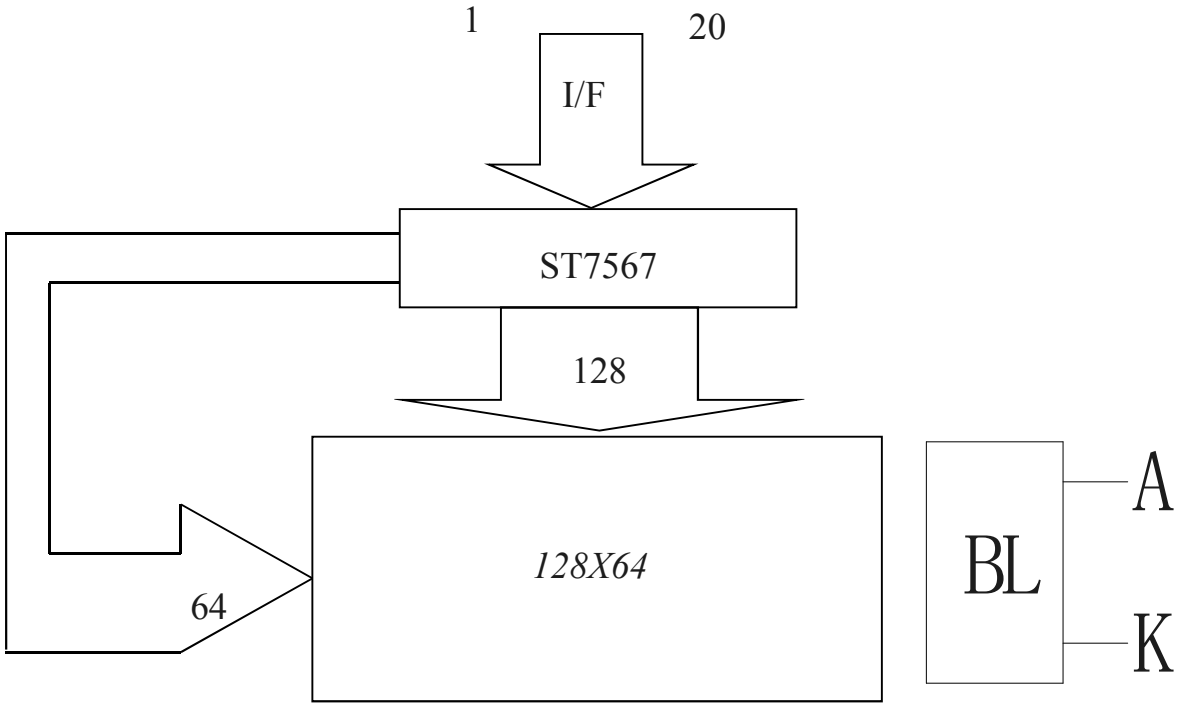
2.0 OUTLINE DRAWING

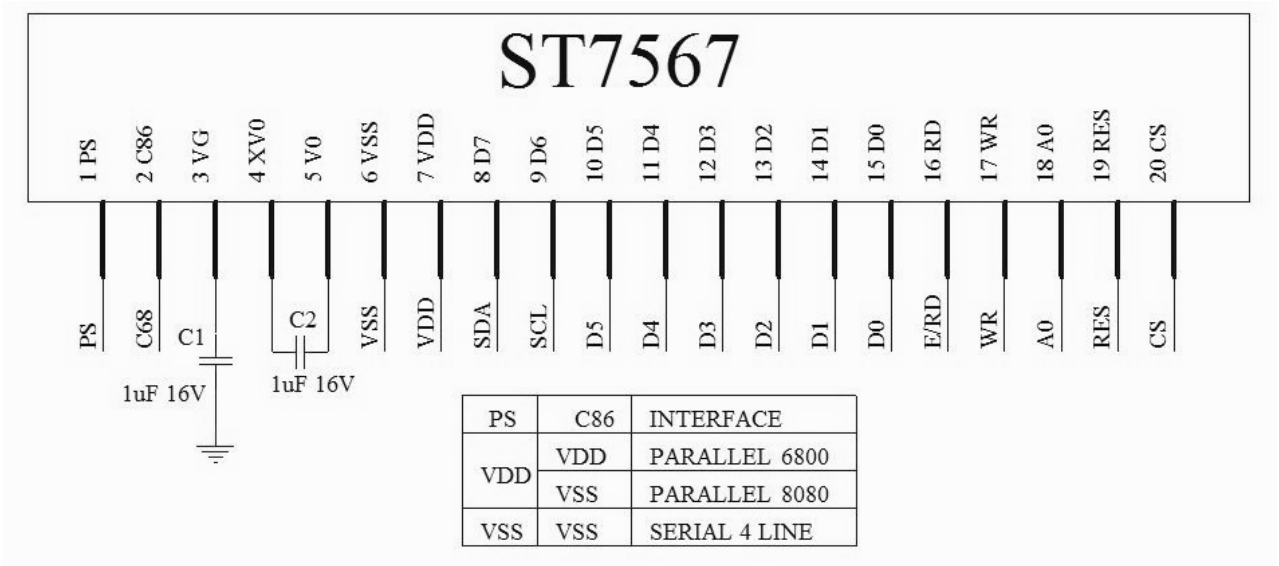


3.0 INTERFACE PIN DESCRIPTION

Pin No.	Symbol	Pin Description
1	PS	Parallel/serial dta input select input pin in parallel mode
2	C86	Microprocessor interface select input pin in parallel mode
3	VG	VG is the LCD driving voltage for segment circuits at positive frame
4	XV0	XV0 is the LCD driving voltage for common circuits at positive frame
5	V0	V0 is the LCD driving voltage for common circuits at negative frame
6	VSS	Ground
7	VDD	Power supply（+3.0）
8-15	D7-D0	Data bus
16	RD	Read select signal
17	WR	Write select signal input
18	A0	Data or command select signal input
19	RES	A reset pin.
20	CS	Chip select signal input(low active)

4.0 BLOCK DIAGRAM





PS	C86	INTERFACE
VDD	VDD	PARALLEL 6800
	VSS	PARALLEL 8080
VSS	VSS	SERIAL 4 LINE

5.0 OPERATING PRINCIPLE & DRIVING METHOD

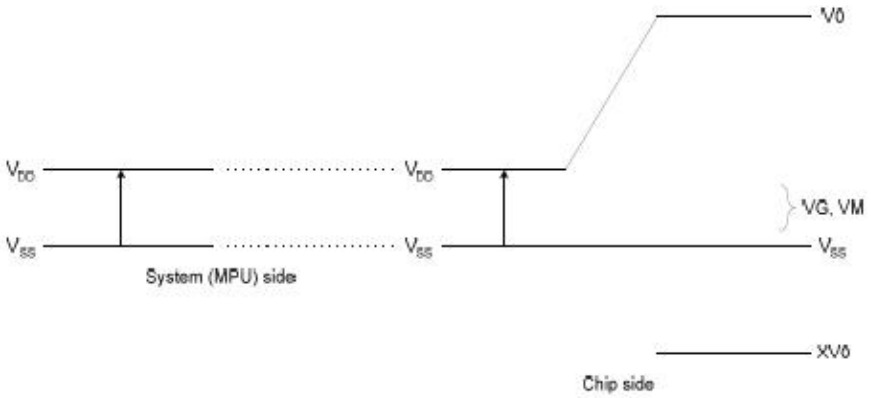
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4) Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Test	0	0	1	1	1	1	1	1	1	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

6.0 ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 3.6	V
Analog Power supply voltage	VDD2, VDD3	-0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0	-0.3 ~ 16	V
LCD Power supply voltage	VG	-0.3 ~ 3.6	V
LCD Power supply voltage	VM	-0.3 ~ VDD2	V
Input Voltage	Vi	-0.3 ~ VDD1+0.3	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–55 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VDD2 > VG > VM > VSS ≥ XV0

7.0 ELECTRICAL CHARACTERISTICS

VSS=0V; Tamb = -30°C to +85°C; unless otherwise specified.

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.7	—	3.3	V	VDD1
Operating Voltage (2)	VDD2			2.4	—	3.3	V	VDD2
Operating Voltage (3)	VDD3			2.4	—	3.3	V	VDD3
Input High-level Voltage	V_{IHC}			0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}			VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V		0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V		VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}			-1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}			-3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25°C	Vop=8.5V, ΔV=0.85V	—	0.6	0.8	KΩ	COMx
			VG=1.9V, ΔV=0.19V	—	1.3	1.5	KΩ	SEGx
Frame Frequency	FR	Duty=1/65, Vop=8.5V Ta = 25℃		70	75	80	Hz	

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

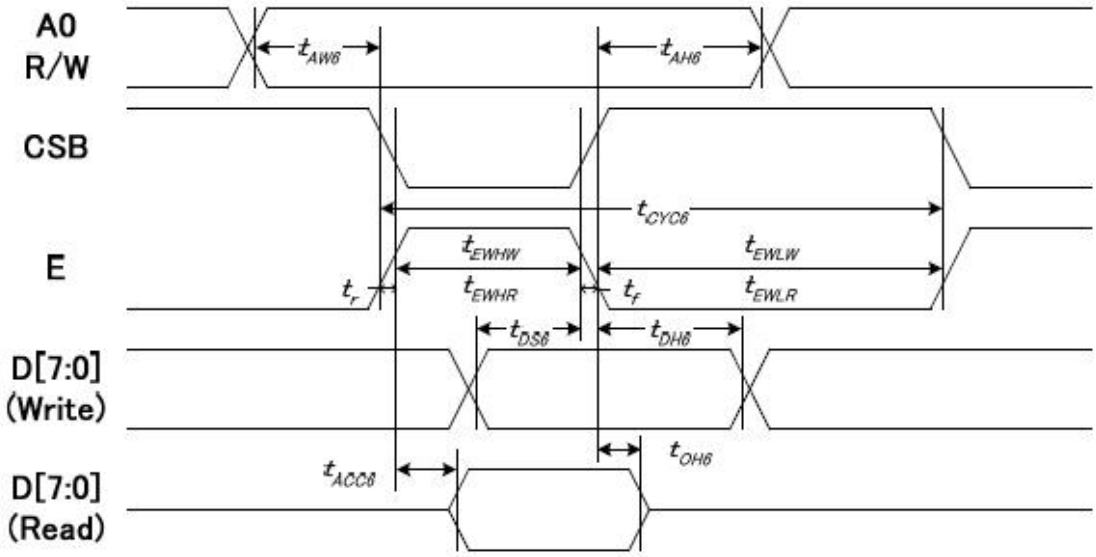
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 V_{OP} = 8.5 V, Bias=1/9 Ta=25°C	—	150	300	μA	
Display OFF	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 V_{OP} = 8.5 V, Bias=1/9 Ta=25°C	—	95	190	uA	
Power Down	ISS	VDD1=VDD2=VDD3=3.0V, Ta=25°C	—	8	16	μA	

Note:

- *The Current Consumption is DC characteristics*

8.0 ELECTRO-OPTICAL CHARACTERISTICS

System Bus Timing for 6800 Series MPU



(VDD1 = 3.3V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		10	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		10	—	
Read data access time		tACC6	CL = 16 pF	—	70	
Read data output disable time		tOH6	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		400	—	
Enable L pulse width (WRITE)		tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	140	
Read data output disable time		tOH6	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25°C)

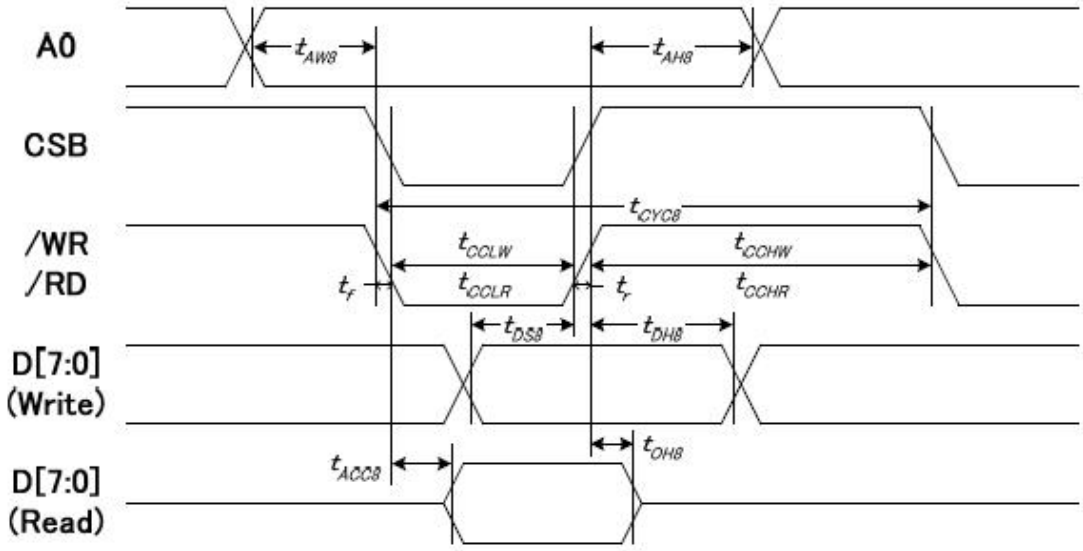
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		640	—	
Enable L pulse width (WRITE)		tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)		tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
Write data setup time	D[7:0]	tDS6		80	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	240	
Read data output disable time		tOH6	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

System Bus Timing for 8080 Series MPU



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		10	—	
System cycle time	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		80	—	
/RD L pulse width (READ)	RD	tCCLR		140	—	
/RD H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	70	
READ Output disable time		tOH8	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		400	—	
/WR L pulse width (WRITE)		tCCLW		220	—	
/WR H pulse width (WRITE)		tCCHW		180	—	
/RD L pulse width (READ)	RD	tCCLR		220	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	140	
READ Output disable time		tOH8	CL = 16 pF	10	100	

(VDD1 = 1.8V , Ta =25°C)

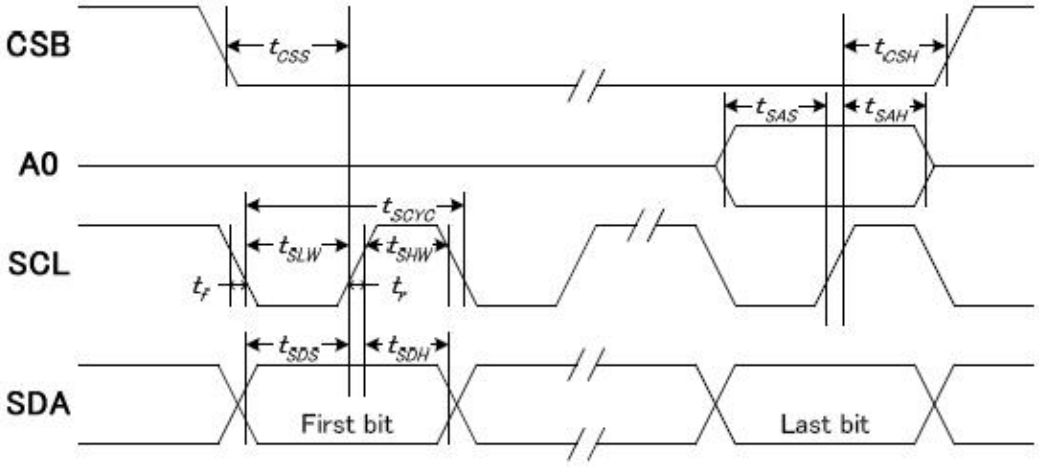
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		640	—	
/WR L pulse width (WRITE)		tCCLW		360	—	
/WR H pulse width (WRITE)		tCCHW		280	—	
/RD L pulse width (READ)	RD	tCCLR		360	—	
/RD H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 16 pF	—	240	
READ Output disable time		tOH8	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

System Bus Timing for 4-Line Serial Interface



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		50	—	ns
SCLK "H" pulse width		tSHW		25	—	
SCLK "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		40	—	

(VDD1 = 2.8V , Ta =25°C)

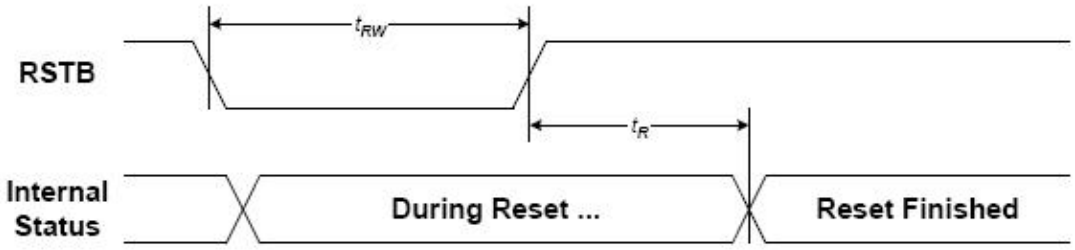
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		100	—	ns
SCLK "H" pulse width		tSHW		50	—	
SCLK "L" pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		60	—	

(VDD1 = 1.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		200	—	ns
SCLK "H" pulse width		tSHW		80	—	
SCLK "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of VDD1 as the standard.

Hardware Reset Timing



(VDD1 = 3.3V , Ta =25˚C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset "L" pulse width	tRW		1.0	—	

(VDD1 = 2.8V , Ta =25˚C)

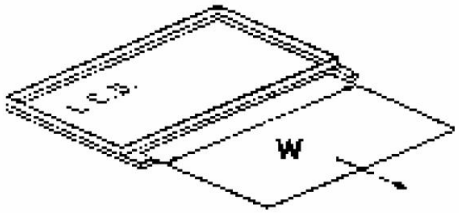
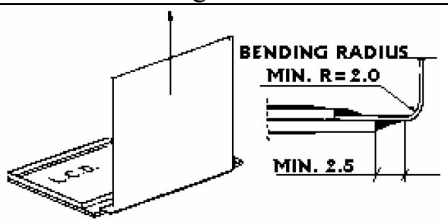
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset "L" pulse width	tRW		2.0	—	

(VDD1 = 1.8V , Ta =25˚C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset "L" pulse width	tRW		3.0	—	

9.0 STANDARD SPECIFICATION FOR RELIABILITY

9.1 Standard specification of Reliability Test

No.	Test Item	Content of Test	Test Condition
1	High temperature operation	Endurance test applying the high storage temperature for a long time.	+70°C for 96Hrs
2	Low temperature operation	Endurance test applying the low storage temperature for a long time.	-20°C for 96Hrs
3	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30 °C for 96hrs
4	High temperature storage	Endurance test applying the low storage temperature for a long time.	+80 °C for 96hrs
5	Damp heat Operation	Endurance test applying the electric stress and temperature / humidity stress to the element for a long time.	+60 °C, 95%RH for 96Hrs
6	Thermal cycles operation	Endurance test applying the thermal shock operation for a long time.	Display on , 2h at -20°C ; shift from - 20°C to + 70°C with gradient of 3°C/min; 2 h at 70°C; shift from +80°C to - 20°C with gradient of 2°C/min , repeated 10 times.
7	ESD test	To check the immunity of display to ESD incurred during storage, handling, maintenance and assembly operation.	Discharge resistance = 2kΩ Discharge capacitance = 150pF Number of discharges = 3times Discharge interval = 3 sec Discharge voltage = ± 2 kV on COG connection interface.
8	FPC pull test	To verify the FPC/ glass connection resistance to pull forces applied to the FPC.	 Keeping the LCD fixed, pull the FPC/FFC with a force F= 40 N for cm width of FPC at glass connection.
9	FPC peel test	To verify the FPC/ glass connection resistance to peel forces applied to the FPC.	 Keeping the LCD fixed, pull the FPC/FFC according to the figure above with a force F= 10 N for cm width of FPC at glass connection. The minimum bending radius has to be 2 mm

Remarks:

1) For operation test, above specification is applicable when test pattern is changing during entire operation test.
2) Inspections after reliability tests are performed when the display temperature resumes back to room temperature.

3) It is a normal characteristic that some display abnormality can be seen during reliability test. If the display abnormality can resume back to normal condition at room temperature within 24hours, there is no permanent destruction over the display. The display still possesses its functionality after reliability tests.

9.2 Failure Judgment Criteria

After the reliability tests above, test sample shall be let return to room temperature and humidity for at least 4 hours before final tests are carried out.

Criterion Item	Failure Judgment Criteria
Electrical characteristic	Electrical short and open.
Mechanical characteristic	Out of mechanical specification
Optical characteristic	Out of the Appearance Standard

10.0 QUALITY ASSURANCE

10.1 Inspection Standard

Item	Contents
Objective	This product inspection standard is intended to provide an inspection guideline for the LCD or LCM products manufactured by the Company.
Scope	Applicable to the inspection criteria of dimension, appearance, functionality etc.for the LCD or LCM products supplied to the customer. Criteria not included in this Inspection Standard will be justified in accordance with any documents agreed upon otherwise.
Inspection Unit	
Inspection System	1： Inspection system includes inspection during production inspection and outgoing product inspection. 2：Process inspection is the inspection for appearance and functionality of the products during the production process. 3： Outgoing inspection is the inspection for the finished products prior to the delivery, based on defined sampling plan.

Inspection Condition	1： Inspection equipments: Equipment and tools used for inspection, measuring and testing during the inspection process. 2：Inspection conditions are described as the following. Distance：40cm between the observer's eyes and the LCD. Viewing angle：according to main viewing direction（MVD）.

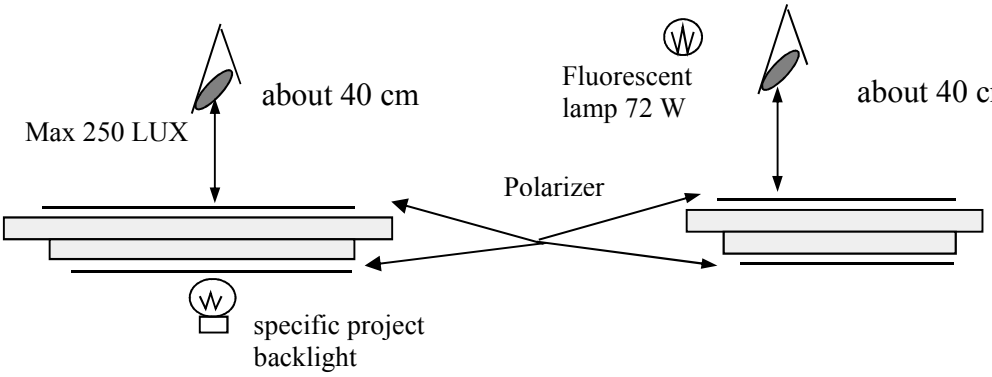


Fig 1
Trasflective or Transmissive LCD/LCM

Fig 2
Reflective LCD/LCM

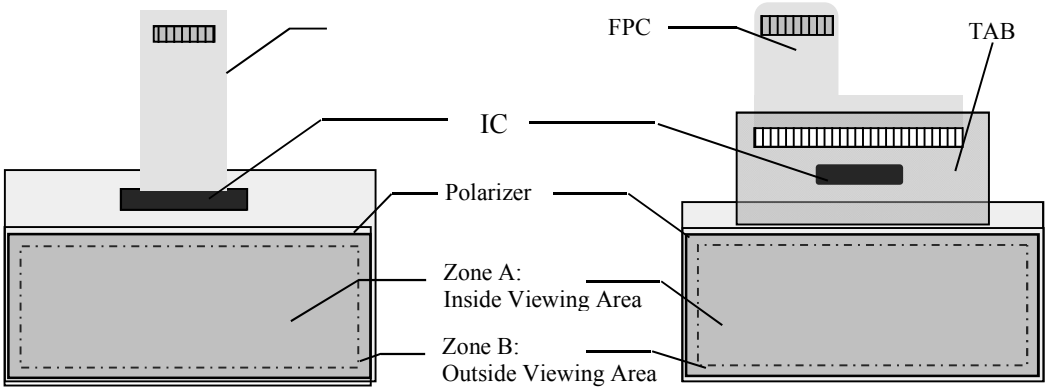
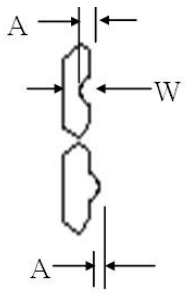
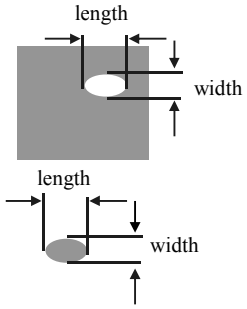


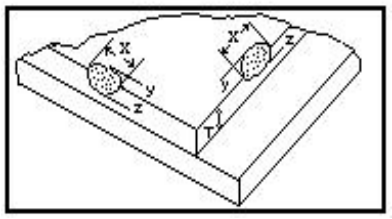
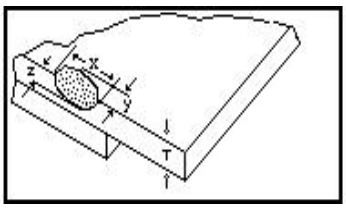
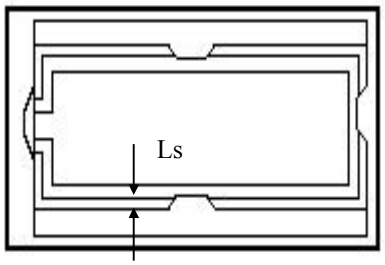
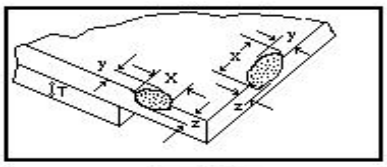
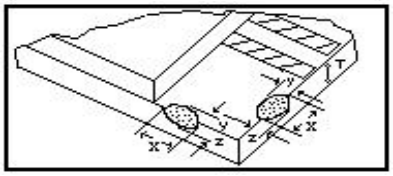
Fig 3
Product Configuration

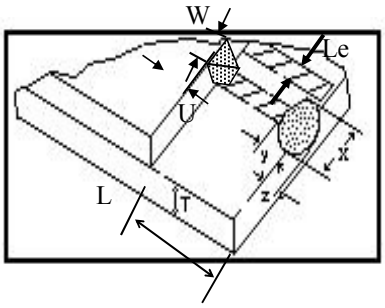
10.2 Acceptance Criteria

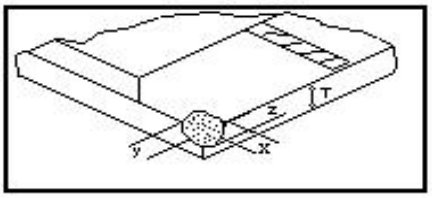
<table>
<tr><th>Inspection Item</th><th>Acceptance/Rejection Criteria</th><th>Defect Classification</th><th>Method</th><th>Applicable Zone</th></tr>
<tr><td>Functional</td><td>1. No display defect is not acceptable.
2. Abnormal display defect is not acceptable.
3. Missing segment and extra segment is not acceptable.
4. Dim contrast or dark contrast is not acceptable.
5. Current consumption (Idd MAX) shall not exceed the limit specified on the MI.
6. Wrong/reversed viewing angle is not acceptable.
7. Uneven contrast or stripe defect shall be in accordance with master sample. (Refer to specified limit sample if applicable)
8. Display character/ pattern shall be referred to the Test Instruction of the related models.</td><td>Major</td><td>Visual</td><td>A</td></tr>
<tr><td>Pattern Deformation</td><td> 

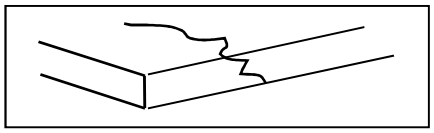
<table>
<tr><th>Size</th><th>Acceptable Number</th></tr>
<tr><td>A≤0.10 or A≤1/4W, whichever is less</td><td>1 per segment
3 per display</td></tr>
<tr><td>A>0.10 or A>1/4W, whichever is less</td><td>Unlimted</td></tr>
</table>
Note: Protrusion shall not cause bridging between adjacent segments</td><td>Major</td><td>Visual
Magnifier</td><td>A</td></tr>
<tr><td>Black or white spots (on pattern), pin hole</td><td> 

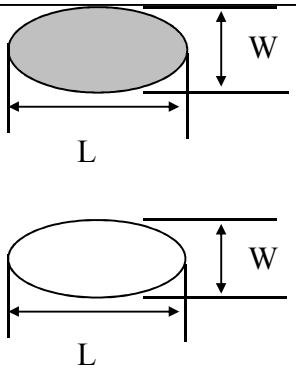
<table>
<tr><th>Size, d (mm)</th><th>Acceptable quantity</th></tr>
<tr><td>d ≤ 0.15</td><td>Unlimited</td></tr>
<tr><td>0.15 < d ≤ 0.25</td><td>1</td></tr>
<tr><td>d > 0.25</td><td>0</td></tr>
<tr><td colspan="2">d = (length + width) / 2</td></tr>
</table>
Note:
Number of spot shall not be more than 1 per each segment.
If 2 spots exist, the distance must be > 20mm between each other</td><td>Minor</td><td>Visual
Magnifier</td><td>A</td></tr>
</table>

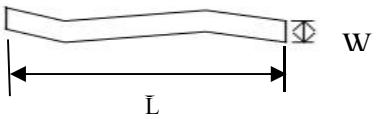
<table>
<tr>
<td>Chip-out</td>
<td>A. General chip-out (for glass edges and glass corner along perimeter seal)
 
 
 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>⩽2.0</td><td>⩽1.5 or ⩽Ls, whichever is less</td><td>⩽1/2t</td></tr>
<tr><td>⩽2.0</td><td>⩽1.0 or ⩽Ls, whichever is less</td><td>⩽t</td></tr>
<tr><td colspan="3">X = length parallel with glass edge.
Y = width perpendicular with glass edge
Z = height of glass
t = single glass thickness</td></tr>
</table>
Note:
Chip out shall not reach the perimeter seal.</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>B</td>
</tr>
<tr>
<td></td>
<td>B： Chip-out at terminal ledge or back of terminal ledge, but no exactly on terminal
 
 
<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤2.0</td><td>≤1.5</td><td>≤1/2t</td></tr>
<tr><td>≤2.0</td><td>≤1.0</td><td>≤t</td></tr>
</table>
Note:
In the event that the distance between the chip-out location and the terminal is less than the width of ITO pad Le, the acceptance criteria of chip-out on terminal shall apply.</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>B</td>
</tr>
</table>

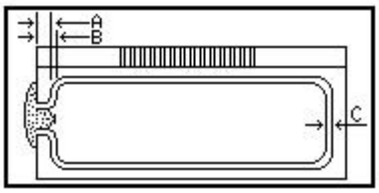
<table>
<tr>
<td></td>
<td>C：Chip-out and protuberance at terminals
 

<table>
<tr><th>W</th><th>U</th></tr>
<tr><td colspan="2">Meet the dimension tolerance of the drawing</td></tr>
</table>
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤0.5 Le
& not bridge two adjacent ITO pads.</td><td>≤0.2L or ≤2.0mm whichever is less</td><td>≤1/2t</td></tr>
</table>
Note:
Chip out and protuberance shall not co-exist on the same ITO pad.
Protuberance is not allowed if affect assembly.</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>B</td>
</tr>
<tr>
<td></td>
<td>D：Chip-out at corner (ITO ledge)
 

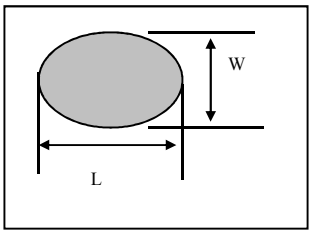
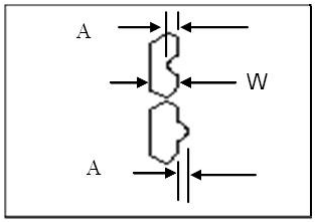
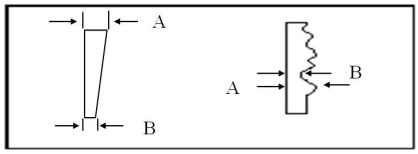
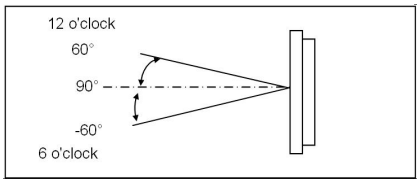
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤2.0</td><td>≤2.0</td><td>≤t</td></tr>
</table></td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>B</td>
</tr>
<tr>
<td>Crack line</td>
<td> 
Crack line is not acceptable.</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A &
B</td>
</tr>
<tr>
<td>Number of Chip-out</td>
<td>Maximum acceptable number of chip-out: 2 defects per LCD; 1 defect on ITO ledge.
Distance between chip-out: > 5mm.</td>
<td>Minor</td>
<td>Visual</td>
<td>B</td>
</tr>
</table>

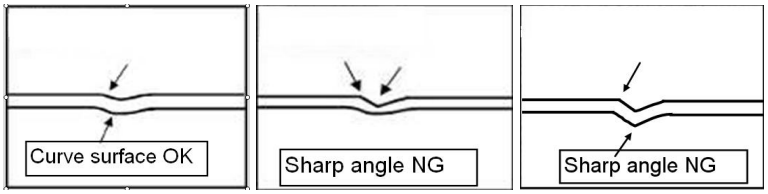
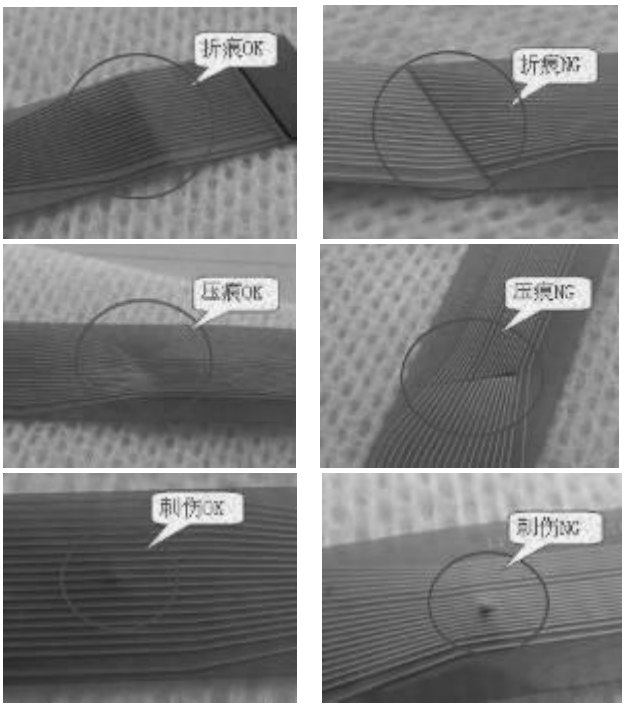
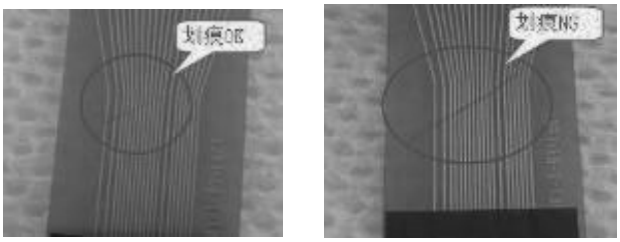
<table>
<tr>
<td>Black spot
White spot
Bubble
Foreign material
Dent</td>
<td>


<table>
<tr><th>D</th><th>Acceptable Number</th></tr>
<tr><td>D≤0.15</td><td>Unlimited</td></tr>
<tr><td>0.15＜D≤0.25</td><td>1</td></tr>
<tr><td>D＞0.25</td><td>0</td></tr>
<tr><td colspan="2">Note: If 2 spots exist, the distance must be > 20mm between each other</td></tr>
</table>
D=（L+W）/2
</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A</td>
</tr>
<tr>
<td>Scratch line
Dark line
Lint</td>
<td>


<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Number</th></tr>
<tr><td>L≤3.0</td><td>W≤0.015</td><td>2</td></tr>
<tr><td>L≤1.5</td><td>W≤0.03</td><td>1</td></tr>
<tr><td></td><td>W＞0.03</td><td>0</td></tr>
</table>
Note: If 2 line defects co-exist, the distance must be > 20mm between each other
</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A</td>
</tr>
<tr>
<td>Endseal</td>
<td>


<table>
<tr><td>A：Length of end-sealant</td></tr>
<tr><td>B：Length of seal mouth</td></tr>
<tr><td>C：Perimeter seal width</td></tr>
</table>
1.Minimum amount of end-sealant filled, A> 1/3 B
2.Maximum amount of end-sealant shall not spread over to Zone A, Viewing Area (VA).
3.Dimension of end seal shall meet the dimension specified on the drawing.
4.Deformation of perimeter seal which result in perimeter seal becoming less than 1/3 C is not acceptable.
</td>
<td>Minor</td>
<td>Visual
Magni
fier</td>
<td>A,B</td>
</tr>
<tr>
<td>Polarizer</td>
<td>Polarizer position shall meet the dimension tolerance indicated on the drawing</td>
<td>Minor</td>
<td>Visual</td>
<td>A,B</td>
</tr>
<tr>
<td>Background color</td>
<td>Background color shall not exceed the range of the limit sample.
Obvious uneven coloration (rainbow) shall not be seen.</td>
<td>Minor</td>
<td>Visual</td>
<td>A</td>
</tr>
<tr>
<td rowspan="6">Ink printing</td>
<td>1. Pattern position on the display shall match the MI/drawing.</td>
<td>Major</td>
<td>Visual</td>
<td rowspan="6">A</td>
</tr>
<tr>
<td>2. Pattern appearance shall match the MI/drawing.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>3. Reverse printing is not acceptable.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>4. Printing color shall match the master sample.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>5. Insufficient ink, blur, missing pattern, broken pattern are not acceptable.</td>
<td>Major</td>
<td>Visual</td>
</tr>
<tr>
<td>6. Angle of the printed pattern, the dimension between the pattern and the glass edge shall meet the dimension on the drawing.</td>
<td>Major</td>
<td>Visual</td>
</tr>
</table>

	7. The printed patterns shall be free of stain, fingeprint and scratch.	Major	Visual Magnifier	
	8. Spot/pinhole on the pattern.  D=（L+W）/2 D ≤0.15: Unlimited 0.15＜D≤0.25: 1 D＞0.25: 0 Note: If 2 spots exist, the distance must be > 20mm between each other	Major	Visual	
	9. Ink pattern deformation  Protrusion ≤0.10 or ≤1/4W, whichever is less, Indentation ≤0.10 or ≤1/4W, whichever is less	Minor	Visual Magnifier	A
	10. Ink line deformation  A-B≤0.15	Minor	Visual Magnifier	A
	11. Pattern misalignment  Dimension must meet the requirement on the drawing For 12 o'clock viewing angle product, light leakage between 90°to 60° shall not be seen. For 6 o'clock viewing angle product, light leakage between 90°to -60° shall not be seen.	Minor	Visual	A
HSC FPC FFC	1. The outer dimension shall meet the MI/drawing.	Minor	Visual	B

	2. FPC、HSC、FFC、shall not have folding/stress/dented mark with sharp angle on the surface.  			
	4.Scratch on FPC、HSC、FFC、TAB shall not damage the PI layer and the conductive traces. 			
	5.Goldfinger of FPC、TAB、FFC shall be free of solder。			
	6.Goldfinger of FPC、TAB、FFC shall be max 5% of area of oxidization and corrosion. 	Major	Visual	B

Stiffening tape Identity Label Identity marking	1. The tape sticking position shall meet the requirement on the MI/drawing. 2. Missing label/tape/marking is not acceptable. 3. The format of identification (including date code and product code) shall meet the requirement (eg. label,color marking, inkjet printing) on the MI/drawing.	Minor	Visual	B
Metal bezel	1. Dimension and specification shall meet the requirment on the MI/drawing.	Major	Visual	B
	2.The lock tab of bezel shall not have wrong bending orientation, missing tab, or crack.	Minor		B
	3.Bezel shall be free of rust, twist, deformation,finger print,oil stain and unknown contamination.	Minor		B

11.0 PRECAUTIONS FOR USING LCD MODULE

11.1 Handing Precautions

11.1.1 The display panel is made of glass and polarizer. Do not subject it to mechanical shock by dropping or impact which may cause chipping especially on the edges.

11.1.2 Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.3 If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with Isopropyl alcohol or ethyl alcohol. Avoid using solvents like acetone (ketene), water, toluene, ethanol to clean the polarizer surface.

11.1.4 Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

11.1.5 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.6 Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion.

11.1.7 Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

11.1.8 NC terminal should be open. Do not connect anything.

11.1.9 If the logic circuit power is off, do not apply the input signals.

11.1.10 Avoid contacting oil and fats.

11.1.11 Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

11.1.12 Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

11.2 Electro-Static Discharge Control

11.2.1 Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

11.2.2 Be sure to ground the body when handling the LCD modules. Tools required for assembling, such as soldering irons, must be properly grounded.

11.2.3 To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions. To reduce the generation of static electricity, be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

11.2.4 The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

11.2.5 When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

11.3 Precaution for soldering to the LCM

11.3.1 Observe the following when soldering lead wire, connector cable and etc. to the LCD module.

- Soldering iron temperature: 300 ~ 350°C.
- Soldering time: ≤ 3 sec.
- Solder: eutectic solder.

Above is a recommended approach based on a 5mm distance between soldering point and pin contact point. Due to different solder composition, actual distance between soldering and contact point, and processing method, it is recommended that customer to study and fine tuning their soldering process parameters accordingly so that the temperature at pin-LCD contact point does not exceed 85°C during soldering..

11.3.2 If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

11.4 Precautions for Operation

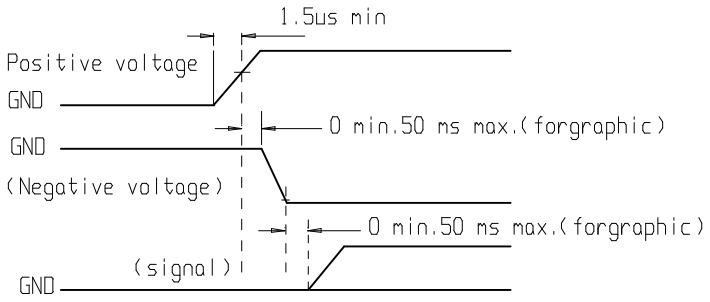
11.4.1 Viewing angle varies with the change of liquid crystal driving voltage (V_O). Adjust V_O to show the best contrast.

11.4.2 Driving the LCD in the voltage above the limit shortens its lifetime.

11.4.3 Response time is greatly delayed at temperature below the operating temperature range. However, it will recover when it returns to the specified temperature range.

11.4.4 If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

11.4.5 When turning the power on, input each signal after the positive/negative voltage becomes stable (below figure is a general illustration where typical value depends on individual product design).



11.5 Storage

11.5.1 When storing LCDs as spares for some years, the following precautions are necessary.

- Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.
- Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

11.5.2 Environmental conditions:

- Do not leave them for more than 168hrs. at 60°C.
- Should not be left for more than 48hrs. at -20°C.

11.6 Safety

11.6.1 It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

11.6.2 If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.