

Amendment history of SSD1309 Specification

Revision	Description of any change	Issued	Effective
0.10 C7KA3 07-Oct-10	Reference from SPD0301 Rev1.0 with following changes: 1. Rename GPIO pin into TR7, LS pin into V_{SS1} (Block Diagram, Pad coordinate, Pin description and application example) 2. Round off die size to 1 d.p. 3. Re-arrange command table sequence according to function 4. Remove note 2 in command 21h 5. Remove note 1 in command A0/A1h 6. Revise command 22h from A[3:0] to A[2:0], from B[3:0] to B[2:0] 7. Remove Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh 8. Remove command description for "Status register Read" 9. Add Content Scrolling software flow example in command description of 2Ch/2Dh Approver list: Product Marketing- Raymond Ho Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong	Janette Wong	12-Oct-10
1.0 C7KA3 13-Oct-10	1. Change to Adv info 2. Remove confidential watermark 3. Add SSD1309UR1 in ordering information (P.11 , P.55) Approver list: Product Marketing- Raymond Ho Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong / Stephen Leung	Ada Ng	14-Oct-10
1.1 C7KA3 19-Jul-11	1. Added Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh in Section 9 & Section 10 2. Revised default value of A[7:4] of command D5h in Table 9-5 from 1000b into 0111b. (P.34) Approver list: Product Marketing- Ringo Lau Design Engineering-Kenneth Lee Product Engineering- Johnkid Lo Quality & Manufacturing- Daniel Ho TE / TPE - Warren Wong / Stephen Leung	Janette Wong	27-Jul-11

SSD1309

Advance Information

128 x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

<http://www.solomon-systech.com>

SSD1309

Rev 1.1

P 1/62

Jul 2011

Copyright © 2011 **Solomon Systech Limited**



Appendix: IC Revision history of SSD1309 Specification

Version	Change Items	Effective Date
0.10	1 st Release	12-Oct-10
1.0	1. Changed to Advance Information 2. Add SSD1309UR1 in ordering information. (P.11 , P.55)	14-Oct-10
1.1	1. Added Command 26h/27h/29h/2Ah/2Eh/2Fh/A3h/DCh in Section 9 & Section 10 (P.28~31, P.33, P.45~48) 2. Revised default value of A[7:4] of command D5h in Table 9-5 from 1000b into 0111b. (P.34)	27-Jul-11

CONTENT

1	GENERAL DESCRIPTION	7
2	FEATURES.....	7
3	ORDERING INFORMATION	7
4	BLOCK DIAGRAM.....	8
5	DIE PAD FLOOR PLAN.....	9
6	PIN ARRANGEMENT	11
6.1	SSD1309UR1 PIN ASSIGNMENT	11
7	PIN DESCRIPTION	13
8	FUNCTIONAL BLOCK DESCRIPTIONS.....	15
8.1	MCU INTERFACE SELECTION.....	15
8.1.1	MCU Parallel 6800-series Interface.....	15
8.1.2	MCU Parallel 8080-series Interface.....	16
8.1.3	MCU Serial Interface (4-wire SPI).....	17
8.1.4	MCU Serial Interface (3-wire SPI).....	18
8.1.5	MCU I ² C Interface.....	19
8.2	COMMAND DECODER	22
8.3	OSCILLATOR CIRCUIT AND DISPLAY TIME GENERATOR.....	22
8.4	RESET CIRCUIT	23
8.5	SEGMENT DRIVERS / COMMON DRIVERS	23
8.6	GRAPHIC DISPLAY DATA RAM (GDDRAM).....	24
8.7	SEG/COM DRIVING BLOCK	25
8.8	POWER ON AND OFF SEQUENCE	26
9	COMMAND TABLE	27
9.1	FUNDAMENTAL COMMAND TABLE	27
9.2	SCROLLING COMMAND TABLE	28
9.3	ADDRESSING SETTING COMMAND TABLE	32
9.4	HARDWARE CONFIGURATION (PANEL RESOLUTION & LAYOUT RELATED) COMMAND TABLE	33
9.5	TIMING & DRIVING SCHEME SETTING COMMAND TABLE	34
9.6	DATA READ / WRITE	35
10	COMMAND DESCRIPTIONS.....	36
10.1	SET LOWER COLUMN START ADDRESS FOR PAGE ADDRESSING MODE (00H~0FH)	36
10.2	SET HIGHER COLUMN START ADDRESS FOR PAGE ADDRESSING MODE (10H~1FH)	36
10.3	SET MEMORY ADDRESSING MODE (20H)	36
10.4	SET COLUMN ADDRESS (21H).....	37
10.5	SET PAGE ADDRESS (22H).....	38
10.6	SET DISPLAY START LINE (40H~7FH)	38
10.7	SET CONTRAST CONTROL FOR BANK0 (81H).....	38
10.8	SET SEGMENT RE-MAP (A0H/A1H).....	38
10.9	ENTIRE DISPLAY ON (A4H/A5H).....	38
10.10	SET NORMAL/INVERSE DISPLAY (A6H/A7H).....	39
10.11	SET MULTIPLEX RATIO (A8H)	39
10.12	SET DISPLAY ON/OFF (AEH/AFH).....	39
10.13	SET PAGE START ADDRESS FOR PAGE ADDRESSING MODE (B0H~B7H)	39
10.14	SET COM OUTPUT SCAN DIRECTION (C0H/C8H).....	39
10.15	SET DISPLAY OFFSET (D3H).....	39
10.16	SET DISPLAY CLOCK DIVIDE RATIO/ OSCILLATOR FREQUENCY (D5H).....	42
10.17	SET PRE-CHARGE PERIOD (D9H)	42
10.18	SET COM PINS HARDWARE CONFIGURATION (DAH).....	42
10.19	SET V _{COMH} DESELECT LEVEL (DBH).....	45

10.20	SET GPIO (DCH).....	45
10.21	NOP (E3H).....	45
10.22	SET COMMAND LOCK (FDH).....	45
10.23	HORIZONTAL SCROLL SETUP (26H/27H).....	45
10.24	CONTINUOUS VERTICAL AND HORIZONTAL SCROLL SETUP (29H/2AH).....	46
10.25	DEACTIVATE SCROLL (2EH).....	48
10.26	ACTIVATE SCROLL (2FH).....	48
10.27	SET VERTICAL SCROLL AREA (A3H).....	48
10.28	CONTENT SCROLL SETUP (2CH/2DH).....	48
11	MAXIMUM RATINGS	51
12	DC CHARACTERISTICS	52
13	AC CHARACTERISTICS	53
14	APPLICATION EXAMPLE	59
15	PACKAGE INFORMATION	60
15.1	SSD1309Z DIE TRAY INFORMATION.....	60
15.2	SSD1309UR1 DETAIL DIMENSION	61

FIGURES

Figure 4-1 : SSD1309 Block Diagram.....	8
Figure 5-1: SSD1309Z Die Drawing	9
Figure 5-2: SSD1309Z alignment mark dimension	9
Figure 6-1 : SSD1309UR1 Pin Assignment	11
Figure 8-1 : Data read back procedure - insertion of dummy read	16
Figure 8-2 : Example of Write procedure in 8080 parallel interface mode	16
Figure 8-3 : Example of Read procedure in 8080 parallel interface mode	16
Figure 8-4 : Display data read back procedure - insertion of dummy read.....	17
Figure 8-5 : Write procedure in 4-wire Serial interface mode	18
Figure 8-6 : Write procedure in 3-wire Serial interface mode	18
Figure 8-7 : I ² C-bus data format	20
Figure 8-8 : Definition of the Start and Stop Condition.....	21
Figure 8-9 : Definition of the acknowledgement condition	21
Figure 8-10 : Definition of the data transfer condition	21
Figure 8-11 : Oscillator Circuit and Display Time Generator	22
Figure 8-12 : Segment Output Waveform in three phases	23
Figure 8-13 : GDDRAM pages structure of SSD1309	24
Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)	24
Figure 8-15 : I _{REF} Current Setting by Resistor Value.....	25
Figure 8-16 : The Power ON sequence.....	26
Figure 8-17 : The Power OFF sequence	26
Figure 10-1 : Address Pointer Movement of Page addressing mode	36
Figure 10-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)	36
Figure 10-3 : Address Pointer Movement of Horizontal addressing mode.....	37
Figure 10-4 : Address Pointer Movement of Vertical addressing mode	37
Figure 10-5: Example of Column and Row Address Pointer Movement (LS pin pulled LOW)	38
Figure 10-6 : Transition between different modes	39
Figure 10-7: Horizontal scroll example: Scroll RIGHT by 1 column.....	45
Figure 10-8: Horizontal scroll example: Scroll LEFT by 1 column	46
Figure 10-9: Horizontal scrolling setup example (LS pin pull LOW)	46
Figure 10-10: Continuous Vertical scrolling setup example (LS pin pull LOW)	47
Figure 10-11: Continuous Vertical and Horizontal scrolling setup example (LS pin pull LOW)	48
Figure 10-12: Content Scrolling example (2Dh, Left Horizontal Scroll by one column).....	49
Figure 13-1 : 6800-series MCU parallel interface characteristics.....	54
Figure 13-2 : 8080-series parallel interface characteristics.....	55
Figure 13-3 : Serial interface characteristics (4-wire SPI).....	56
Figure 13-4 : Serial interface characteristics (3-wire SPI).....	57
Figure 13-5 : I ² C interface Timing characteristics.....	58
Figure 14-1 : Application Example of SSD1309Z.....	59
Figure 15-1: SSD1309Z die tray information	60
Figure 15-2 SSD1309UR1 Detail Dimension.....	61

TABLE

Table 3-1: Ordering Information	7
Table 5-1: SSD1309Z Bump Die Pad Coordinates	10
Table 6-1 : SSD1309UR1 Pin Assignment Table.....	12
Table 7-1 : SSD1309 Pin Description.....	13
Table 7-2 : Bus Interface selection	13
Table 8-1 : MCU interface assignment under different bus interface mode	15
Table 8-2 : Control pins of 6800 interface	15
Table 8-3 : Control pins of 8080 interface	17
Table 8-4 : Control pins of 4-wire Serial interface	17
Table 8-5 : Control pins of 3-wire Serial interface	18
Table 9-1: Fundamental Command Table	27
Table 9-2: Scrolling Command Table.....	28
Table 9-3: Addressing Setting Command Table.....	32
Table 9-4: Hardware Configuration (Panel resolution & layout related) Command Table	33
Table 9-5: Timing & Driving Scheme Setting Command Table	34
Table 9-6 : Read Command Table	35
Table 9-7 : Address increment table (Automatic).....	35
Table 10-1: Example of Set Display Offset and Display Start Line without Remap	40
Table 10-2: Example of Set Display Offset and Display Start Line with Remap	41
Table 10-3 : COM Pins Hardware Configuration	42
Table 10-4 : Content Scrolling software flow example (Page addressing mode – command 20h, 02h).....	49
Table 10-5 : Content Scrolling setting example (Vertical addressing mode – command 20h, 01h).....	50
Table 11-1 : Maximum Ratings (Voltage Referenced to V _{SS})	51
Table 12-1 : DC Characteristics.....	52
Table 13-1 : AC Characteristics.....	53
Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics	54
Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics	55
Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)	56
Table 13-5 : Serial Interface Timing Characteristics (3-wire SPI)	57
Table 13-6 : I ² C Interface Timing Characteristics	58

1 GENERAL DESCRIPTION

SSD1309 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1309 embeds with contrast control, display RAM and oscillator, which reduces the number of external components and power consumption. It has 256-step brightness control. Data/Commands are sent from general MCU through the hardware selectable 6800/8080 series compatible Parallel Interface, I²C interface or Serial Peripheral Interface. It is suitable for many compact portable applications, such as mobile phone sub-display, MP3 player and calculator, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
 - V_{DD} = 1.65V ~ 3.3V for IC logic
 - V_{CC} = 7.0V ~ 16.0V for Panel driving
- For matrix display
 - OLED driving output voltage, 16V maximum
 - Segment maximum source current: 320uA
 - Common maximum sink current: 40mA
 - 256 step contrast brightness current control
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
 - 8-bit 6800/8080-series parallel interface
 - 3 / 4 wire Serial Peripheral Interface
 - I²C Interface
- Screen saving infinite content scrolling function
- Programmable Frame Rate
- Programmable Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- On-Chip Oscillator
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

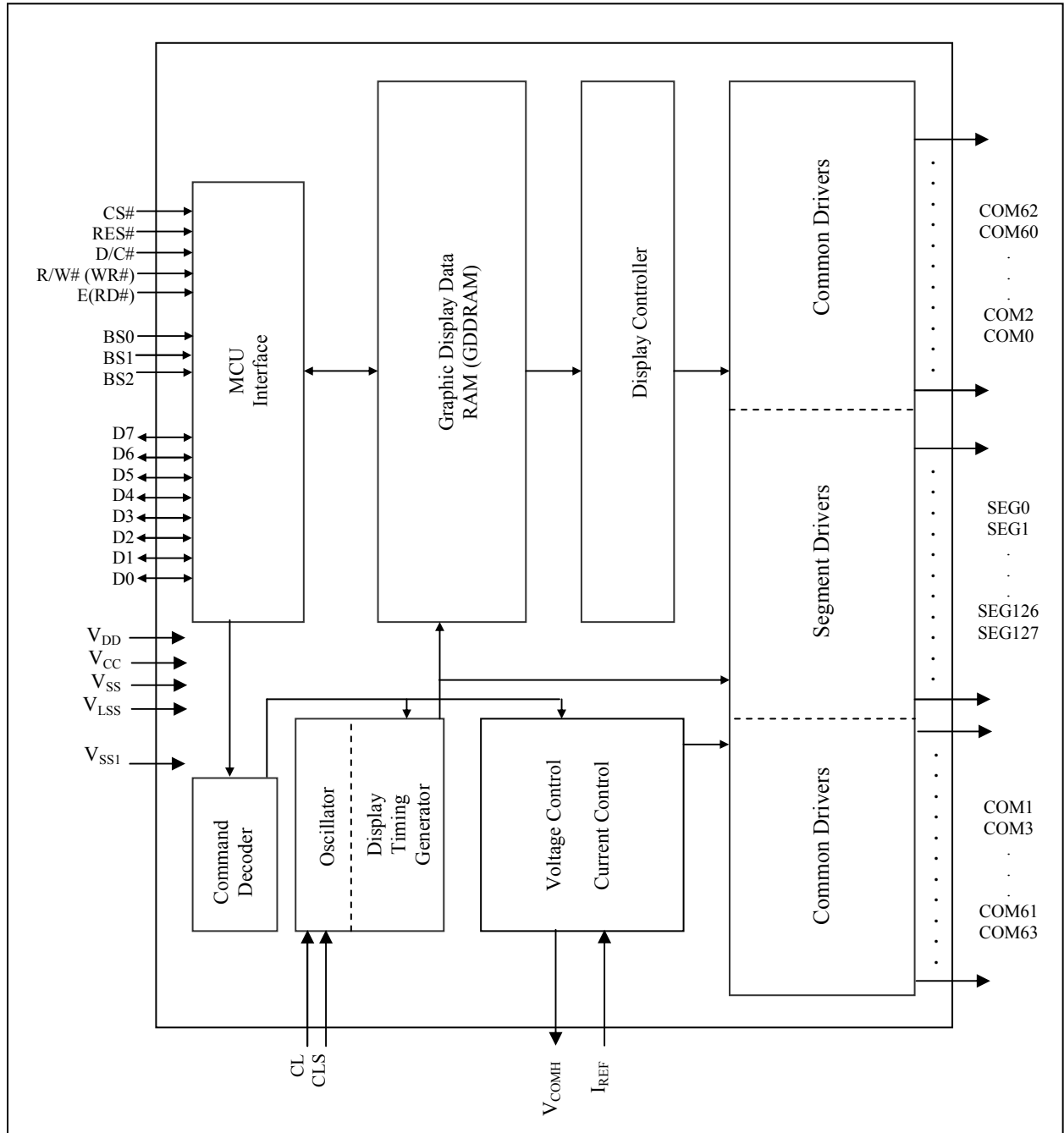
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1309Z	128	64	COG	Page 9	<ul style="list-style-type: none"> ○ Min SEG pad pitch : 37.5um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 60 um ○ Die thickness : 300 +/- 15 um
SSD1309UR1	128	64	COF	Page 11,61	<ul style="list-style-type: none"> ○35mm film, 4 sprocket hole ○Hot bar type COF ○8-bit 80 / 8-bit 68 / SPI / I2C interface ○SEG lead pitch 0.120mm x 0.998 =0.11976mm ○COM lead pitch 0.120mm x 0.998 =0.11976mm

4 BLOCK DIAGRAM

Figure 4-1 : SSD1309 Block Diagram



5 DIE PAD FLOOR PLAN

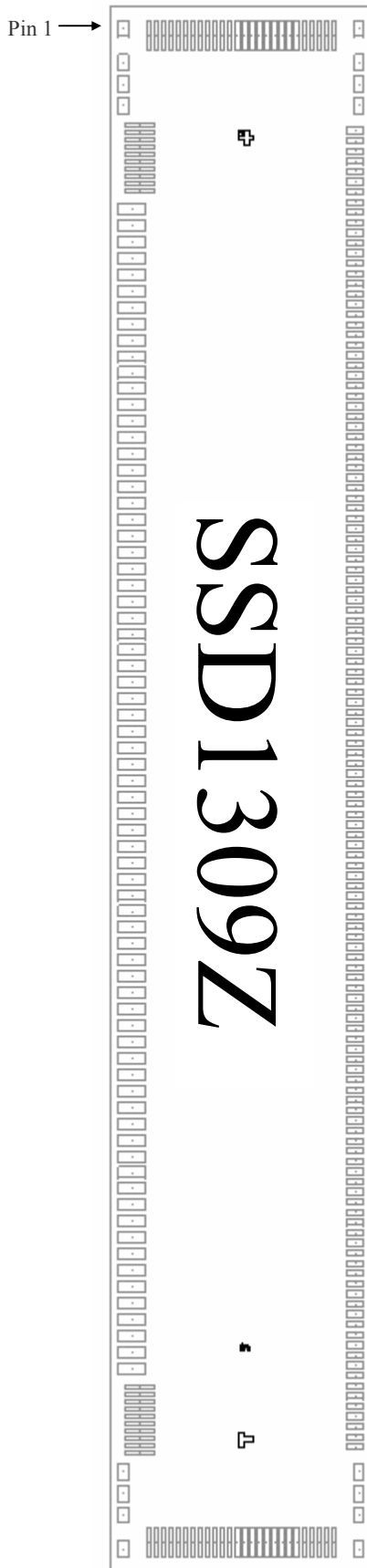


Figure 5-1: SSD1309Z Die Drawing

Die size (after sawing)	$5.8 \pm 0.05\text{mm} \times 1.0 \pm 0.05\text{mm}$
Die thickness	$300 \pm 15\mu\text{m}$
Min I/O pad pitch	60 μm
Min SEG pad pitch	37.5 μm
Min COM pad pitch	27 μm
Bump height	Nominal 12 μm

Bump size		
Pad#	X[μm]	Y[μm]
1~4, 97~100, 127~130, 261~264	59	35
5~14, 87~96	15	108
101~126, 265~290	108	15
15~86	40	100
131~260	22	64

Alignment mark	Position	Size
+ shape	(-2392.2, 18.8)	56.25 $\mu\text{m} \times 56.25\mu\text{m}$
T shape	(2392.2, 18.8)	56.25 $\mu\text{m} \times 56.25\mu\text{m}$
SSL Logo	(2055, 20)	-

(For details dimension please see Figure 5-2)

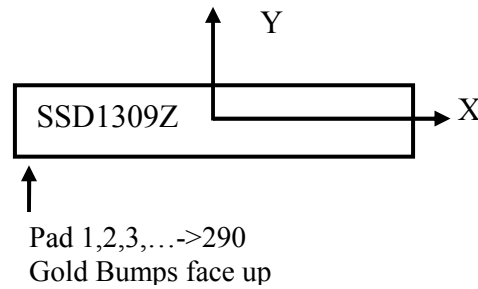


Figure 5-2: SSD1309Z alignment mark dimension

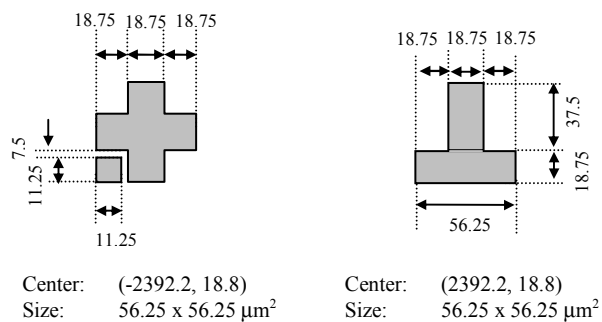


Table 5-1: SSD1309Z Bump Die Pad Coordinates

Pin number	Pin name	X	Y	Pin number	Pin name	X	Y	Pin number	Pin name	X	Y	Pin number	Pin name	X	Y
1	VCOMH	-2794.52	-431.5	81	VSS	1830	-399	161	SEG29	1293.75	417	241	SEG109	-1706.25	417
2	VCOMH	-2698.32	-431.5	82	TR3	1890	-399	162	SEG30	1256.25	417	242	SEG110	-1743.75	417
3	VCOMH	-2589.32	-431.5	83	TR2	1950	-399	163	SEG31	1218.75	417	243	SEG111	-1781.25	417
4	VCOMH	-2510.32	-431.5	84	TR1	2010	-399	164	SEG32	1181.25	417	244	SEG112	-1818.75	417
5	VLSS	-2439.76	-371.02	85	TR0	2070	-399	165	SEG33	1143.75	417	245	SEG113	-1856.25	417
6	COM66	-2412.76	-371.02	86	VCC	2130	-399	166	SEG34	1106.25	417	246	SEG114	-1893.75	417
7	COM67	-2385.76	-371.02	87	VCOMH	2196.76	-371.02	167	SEG35	1068.75	417	247	SEG115	-1931.25	417
8	COM68	-2358.76	-371.02	88	COM81	2223.76	-371.02	168	SEG36	1031.25	417	248	SEG116	-1968.75	417
9	COM69	-2331.76	-371.02	89	COM80	2250.76	-371.02	169	SEG37	993.75	417	249	SEG117	-2006.25	417
10	COM60	-2304.76	-371.02	90	COM29	2277.76	-371.02	170	SEG38	956.25	417	250	SEG118	-2043.75	417
11	COM61	-2277.76	-371.02	91	COM28	2304.76	-371.02	171	SEG39	918.75	417	251	SEG119	-2081.25	417
12	COM62	-2250.76	-371.02	92	COM27	2331.76	-371.02	172	SEG40	881.25	417	252	SEG120	-2118.75	417
13	COM63	-2223.76	-371.02	93	COM26	2358.76	-371.02	173	SEG41	843.75	417	253	SEG121	-2156.25	417
14	VCOMH	-2196.76	-371.02	94	COM25	2385.76	-371.02	174	SEG42	806.25	417	254	SEG122	-2193.75	417
15	NC	-2130	-399	95	COM24	2412.76	-371.02	175	SEG43	768.75	417	255	SEG123	-2231.25	417
16	VLSS	-2070	-399	96	VLSS	2439.76	-371.02	176	SEG44	731.25	417	256	SEG124	-2268.75	417
17	VLSS	-2010	-399	97	VCOMH	2510.32	-431.5	177	SEG45	693.75	417	257	SEG125	-2306.25	417
18	VLSS	-1950	-399	98	VCOMH	2589.32	-431.5	178	SEG46	656.25	417	258	SEG126	-2343.75	417
19	NC	-1890	-399	99	VCOMH	2668.32	-431.5	179	SEG47	618.75	417	259	SEG127	-2381.25	417
20	VOC	-1830	-399	100	VCOMH	2794.52	-431.5	180	SEG48	581.25	417	260	VOC	-2418.75	417
21	VCC	-1770	-399	101	VCOMH	2770.02	-337.5	181	SEG49	543.75	417	261	VCC	-2510.32	431.5
22	VCC	-1710	-399	102	COM23	2770.02	-310.5	182	SEG50	506.25	417	262	VCC	-2589.32	431.5
23	VCC	-1650	-399	103	COM22	2770.02	-283.5	183	SEG51	468.75	417	263	VCC	-2668.32	431.5
24	VCOMH	-1590	-399	104	COM21	2770.02	-256.5	184	SEG52	431.25	417	264	VCOMH	-2794.52	431.5
25	VCOMH	-1530	-399	105	COM20	2770.02	-229.5	185	SEG53	393.75	417	265	VSS	-2770.02	337.5
26	VCOMH	-1470	-399	106	COM19	2770.02	-202.5	186	SEG54	356.25	417	266	COM62	-2770.02	310.5
27	VCOMH	-1410	-399	107	COM18	2770.02	-175.5	187	SEG55	318.75	417	267	COM63	-2770.02	283.5
28	NC	-1350	-399	108	COM17	2770.02	-148.5	188	SEG56	281.25	417	268	COM64	-2770.02	256.5
29	VSS	-1290	-399	109	COM16	2770.02	-121.5	189	SEG57	243.75	417	269	COM65	-2770.02	229.5
30	VSS	-1230	-399	110	COM15	2770.02	-94.5	190	SEG58	206.25	417	270	COM66	-2770.02	202.5
31	VSS	-1170	-399	111	COM14	2770.02	-67.5	191	SEG59	168.75	417	271	COM67	-2770.02	175.5
32	VDD	-1110	-399	112	COM13	2770.02	-40.5	192	SEG60	131.25	417	272	COM68	-2770.02	148.5
33	VDD	-1050	-399	113	COM12	2770.02	-13.5	193	SEG61	93.75	417	273	COM69	-2770.02	121.5
34	VDD	-990	-399	114	COM11	2770.02	13.5	194	SEG62	56.25	417	274	COM40	-2770.02	94.5
35	BS0	-930	-399	115	COM10	2770.02	40.5	195	SEG63	18.75	417	275	COM41	-2770.02	67.5
36	VSS	-870	-399	116	COM9	2770.02	67.5	196	SEG64	-18.75	417	276	COM42	-2770.02	40.5
37	BS1	-810	-399	117	COM8	2770.02	94.5	197	SEG65	-56.25	417	277	COM43	-2770.02	13.5
38	VDD	-750	-399	118	COM7	2770.02	121.5	198	SEG66	-93.75	417	278	COM44	-2770.02	-13.5
39	BS2	-690	-399	119	COM6	2770.02	148.5	199	SEG67	-131.25	417	279	COM45	-2770.02	-40.5
40	VSS	-630	-399	120	COM5	2770.02	175.5	200	SEG68	-168.75	417	280	COM46	-2770.02	-67.5
41	TR7	-570	-399	121	COM4	2770.02	202.5	201	SEG69	-206.25	417	281	COM47	-2770.02	-94.5
42	VSS1	-510	-399	122	COM3	2770.02	229.5	202	SEG70	-243.75	417	282	COM48	-2770.02	-121.5
43	CL	-450	-399	123	COM2	2770.02	256.5	203	SEG71	-281.25	417	283	COM49	-2770.02	-148.5
44	VSS	-390	-399	124	COM1	2770.02	283.5	204	SEG72	-318.75	417	284	COM50	-2770.02	-175.5
45	CS#	-330	-399	125	COM0	2770.02	310.5	205	SEG73	-356.25	417	285	COM51	-2770.02	-202.5
46	RES#	-270	-399	126	VSS	2770.02	337.5	206	SEG74	-393.75	417	286	COM62	-2770.02	-229.5
47	DC#	-210	-399	127	VCOMH	2794.52	431.5	207	SEG75	-431.25	417	287	COM63	-2770.02	-256.5
48	VSS	-150	-399	128	VCC	2668.32	431.5	208	SEG76	-468.75	417	288	COM64	-2770.02	-283.5
49	RW# WR#	-90	-399	129	VCC	2589.32	431.5	209	SEG77	-506.25	417	289	COM65	-2770.02	-310.5
50	E(RD#)	-30	-399	130	VCC	2510.32	431.5	210	SEG78	-543.75	417	290	VCOMH	-2770.02	-337.5
51	D0	30	-399	131	VCC	2418.75	417	211	SEG79	-581.25	417				
52	D1	90	-399	132	SEG0	2381.25	417	212	SEG80	-618.75	417				
53	D2	150	-399	133	SEG1	2343.75	417	213	SEG81	-656.25	417				
54	D3	210	-399	134	SEG2	2306.25	417	214	SEG82	-693.75	417				
55	VSS	270	-399	135	SEG3	2268.75	417	215	SEG83	-731.25	417				
56	D4	330	-399	136	SEG4	2231.25	417	216	SEG84	-768.75	417				
57	D5	390	-399	137	SEG5	2193.75	417	217	SEG85	-806.25	417				
58	D6	450	-399	138	SEG6	2156.25	417	218	SEG86	-843.75	417				
59	D7	510	-399	139	SEG7	2118.75	417	219	SEG87	-881.25	417				
60	IREF	570	-399	140	SEG8	2081.25	417	220	SEG88	-918.75	417				
61	VSS	630	-399	141	SEG9	2043.75	417	221	SEG89	-956.25	417				
62	CLS	690	-399	142	SEG10	2006.25	417	222	SEG90	-993.75	417				
63	VDD	750	-399	143	SEG11	1968.75	417	223	SEG91	-1031.25	417				
64	VDD	810	-399	144	SEG12	1931.25	417	224	SEG92	-1068.75	417				
65	VCOMH	870	-399	145	SEG13	1893.75	417	225	SEG93	-1106.25	417				
66	VCOMH	930	-399	146	SEG14	1856.25	417	226	SEG94	-1143.75	417				
67	VCOMH	990	-399	147	SEG15	1818.75	417	227	SEG95	-1181.25	417				
68	VCOMH	1050	-399	148	SEG16	1781.25	417	228	SEG96	-1218.75	417				
69	VCC	1110	-399	149	SEG17	1743.75	417	229	SEG97	-1256.25	417				
70	VCC	1170	-399	150	SEG18	1706.25	417	230	SEG98	-1293.75	417				
71	VCC	1230	-399	151	SEG19	1668.75	417	231	SEG99	-1331.25	417				
72	VCC	1290	-399	152	SEG20	1631.25	417	232	SEG100	-1368.75	417				
73	VCC	1350	-399	153	SEG21	1593.75	417	233	SEG101	-1406.25	417				
74	NC	1410	-399	154	SEG22	1556.25	417	234	SEG102	-1443.75	417				
75	VLSS	1470	-399	155	SEG23	1518.75	417	235	SEG103	-1481.25	417				
76	VLSS	1530	-399	156	SEG24	1481.25	417	236	SEG104	-1518.75	417				
77	VLSS	1590	-399	157	SEG25	1443.75	417	237	SEG105	-1556.25	417				
78	TR6	1650	-399	158	SEG26	1406.25	417	238	SEG106	-1593.75	417				
79	TR5	1710	-399	159	SEG27	1368.75	417	239	SEG107	-1631.25	417				
80	TR4	1770	-399	160	SEG28	1331.25	417	240	SEG108	-1668.75	417				

6 PIN ARRANGEMENT

6.1 SSD1309UR1 pin assignment

Figure 6-1 : SSD1309UR1 Pin Assignment

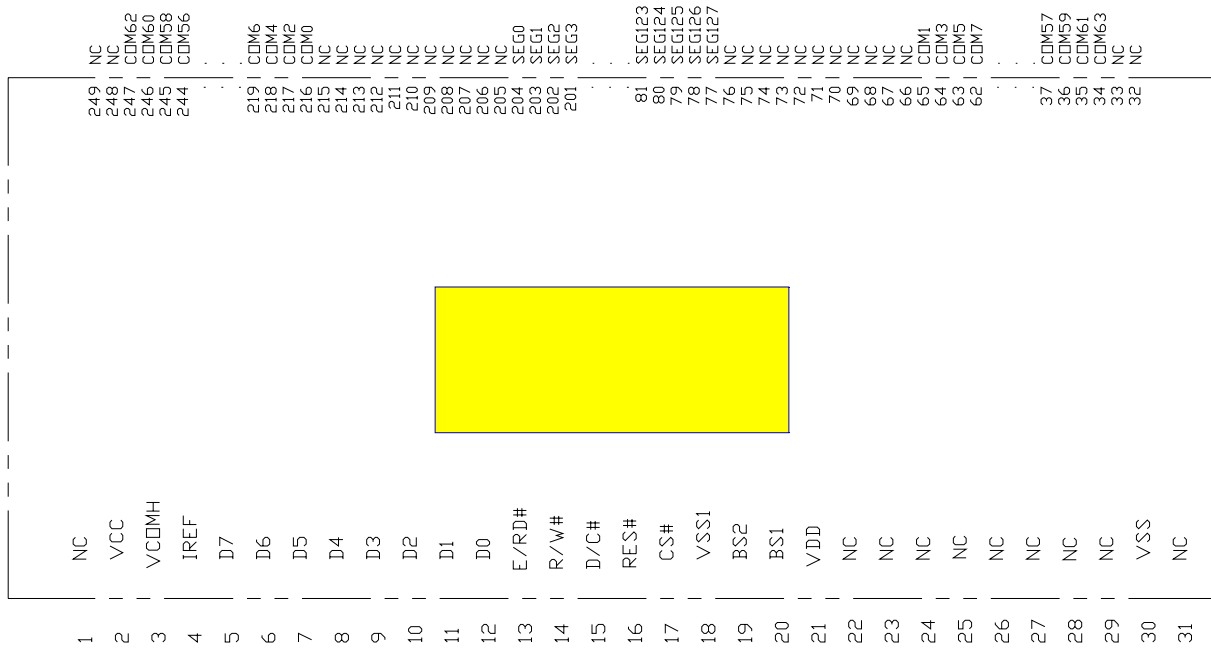


Table 6-1 : SSD1309UR1 Pin Assignment Table

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	81	SEG123	161	SEG43	241	COM50
2	VCC	82	SEG122	162	SEG42	242	COM52
3	VCOMH	83	SEG121	163	SEG41	243	COM54
4	IREF	84	SEG120	164	SEG40	244	COM56
5	D7	85	SEG119	165	SEG39	245	COM58
6	D6	86	SEG118	166	SEG38	246	COM60
7	D5	87	SEG117	167	SEG37	247	COM62
8	D4	88	SEG116	168	SEG36	248	NC
9	D3	89	SEG115	169	SEG35	249	NC
10	D2	90	SEG114	170	SEG34		
11	D1	91	SEG113	171	SEG33		
12	D0	92	SEG112	172	SEG32		
13	E(RD#)	93	SEG111	173	SEG31		
14	R/W#	94	SEG110	174	SEG30		
15	D/C#	95	SEG109	175	SEG29		
16	RES#	96	SEG108	176	SEG28		
17	CS#	97	SEG107	177	SEG27		
18	VSS1	98	SEG106	178	SEG26		
19	BS2	99	SEG105	179	SEG25		
20	BS1	100	SEG104	180	SEG24		
21	VDD	101	SEG103	181	SEG23		
22	NC	102	SEG102	182	SEG22		
23	NC	103	SEG101	183	SEG21		
24	NC	104	SEG100	184	SEG20		
25	NC	105	SEG99	185	SEG19		
26	NC	106	SEG98	186	SEG18		
27	NC	107	SEG97	187	SEG17		
28	NC	108	SEG96	188	SEG16		
29	NC	109	SEG95	189	SEG15		
30	VSS	110	SEG94	190	SEG14		
31	NC	111	SEG93	191	SEG13		
32	NC	112	SEG92	192	SEG12		
33	NC	113	SEG91	193	SEG11		
34	COM63	114	SEG90	194	SEG10		
35	COM61	115	SEG89	195	SEG9		
36	COM59	116	SEG88	196	SEG8		
37	COM57	117	SEG87	197	SEG7		
38	COM55	118	SEG86	198	SEG6		
39	COM53	119	SEG85	199	SEG5		
40	COM51	120	SEG84	200	SEG4		
41	COM49	121	SEG83	201	SEG3		
42	COM47	122	SEG82	202	SEG2		
43	COM45	123	SEG81	203	SEG1		
44	COM43	124	SEG80	204	SEG0		
45	COM41	125	SEG79	205	NC		
46	COM39	126	SEG78	206	NC		
47	COM37	127	SEG77	207	NC		
48	COM35	128	SEG76	208	NC		
49	COM33	129	SEG75	209	NC		
50	COM31	130	SEG74	210	NC		
51	COM29	131	SEG73	211	NC		
52	COM27	132	SEG72	212	NC		
53	COM25	133	SEG71	213	NC		
54	COM23	134	SEG70	214	NC		
55	COM21	135	SEG69	215	NC		
56	COM19	136	SEG68	216	COM0		
57	COM17	137	SEG67	217	COM2		
58	COM15	138	SEG66	218	COM4		
59	COM13	139	SEG65	219	COM6		
60	COM11	140	SEG64	220	COM8		
61	COM9	141	SEG63	221	COM10		
62	COM7	142	SEG62	222	COM12		
63	COM5	143	SEG61	223	COM14		
64	COM3	144	SEG60	224	COM16		
65	COM1	145	SEG59	225	COM18		
66	NC	146	SEG58	226	COM20		
67	NC	147	SEG57	227	COM22		
68	NC	148	SEG56	228	COM24		
69	NC	149	SEG55	229	COM26		
70	NC	150	SEG54	230	COM28		
71	NC	151	SEG53	231	COM30		
72	NC	152	SEG52	232	COM32		
73	NC	153	SEG51	233	COM34		
74	NC	154	SEG50	234	COM36		
75	NC	155	SEG49	235	COM38		
76	NC	156	SEG48	236	COM40		
77	SEG127	157	SEG47	237	COM42		
78	SEG126	158	SEG46	238	COM44		
79	SEG125	159	SEG45	239	COM46		
80	SEG124	160	SEG44	240	COM48		

7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O = Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DD}
P = Power pin	

Table 7-1 : SSD1309 Pin Description

Pin Name	Pin Type	Description												
V_{DD}	P	Power supply pin for core logic operation.												
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.												
V_{SS}	P	Ground pin. It must be connected to external ground.												
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.												
V_{SS1}	-	Reserved Pin. It must be connected to external ground.												
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS} .												
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. <div style="text-align: center;"> Table 7-2 : Bus Interface selection <table border="1" style="margin: auto;"> <thead> <tr> <th>BS[2:0]</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>4 line SPI</td> </tr> <tr> <td>001</td> <td>3 line SPI</td> </tr> <tr> <td>010</td> <td>I²C</td> </tr> <tr> <td>110</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>100</td> <td>8-bit 6800 parallel</td> </tr> </tbody> </table> </div> <p>Note ⁽¹⁾ 0 is connected to V_{SS} ⁽²⁾ 1 is connected to V_{DD}</p>	BS[2:0]	Interface	000	4 line SPI	001	3 line SPI	010	I ² C	110	8-bit 8080 parallel	100	8-bit 6800 parallel
BS[2:0]	Interface													
000	4 line SPI													
001	3 line SPI													
010	I ² C													
110	8-bit 8080 parallel													
100	8-bit 6800 parallel													
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to Figure 8-15 for the details of resistor value												
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS} . When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.												
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.												

Pin Name	Pin Type	Description
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I ² C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V _{SS} . For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams Figure 13-1 to Figure 13-5
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to V _{SS} .
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I ² C interface is selected, this pin must be connected to V _{SS} .
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I ² C mode is selected, D2, D1 should be tied together and serve as SDA _{out} , SDA _{in} in application and D0 is the serial clock input, SCL.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are V _{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
TR[7:0]	-	Reserved pin and is recommended to keep it float.
NC	-	This is dummy pin. Do not group or short NC pins together.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface selection

SSD1309 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-2 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#	
4-wire SPI	Tie LOW				NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#	
I ² C	Tie LOW				SDA _{OUT}	SDA _{IN}	SCL	Tie LOW			SA0	RES#	

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note

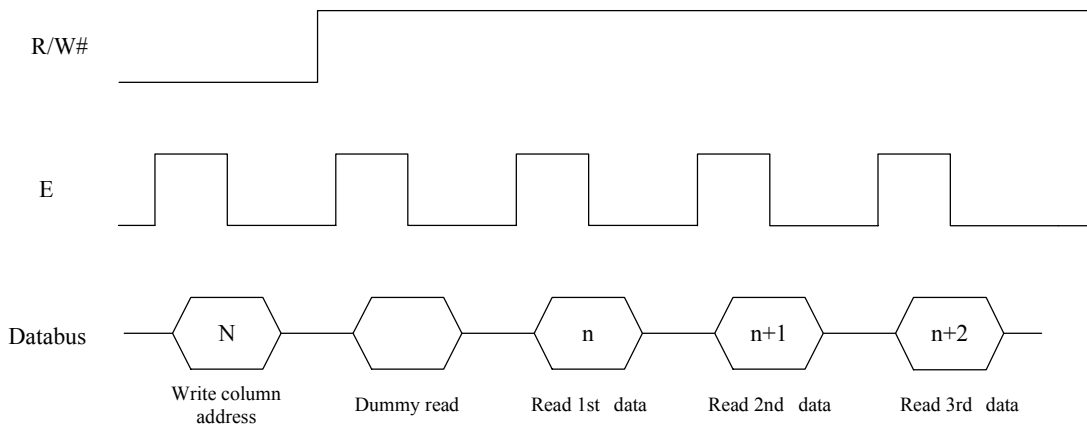
⁽¹⁾ ↓ stands for falling edge of signal

H stands for HIGH in signal

L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

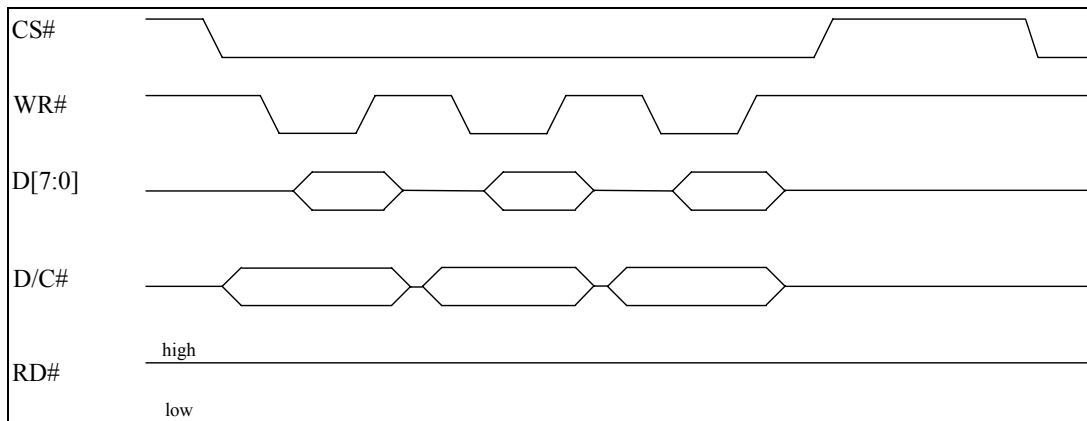


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

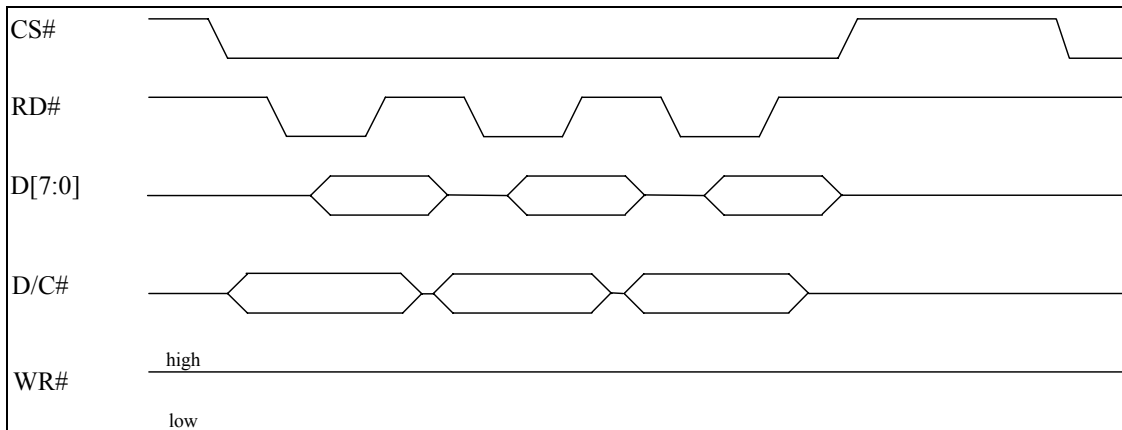


Table 8-3 : Control pins of 8080 interface

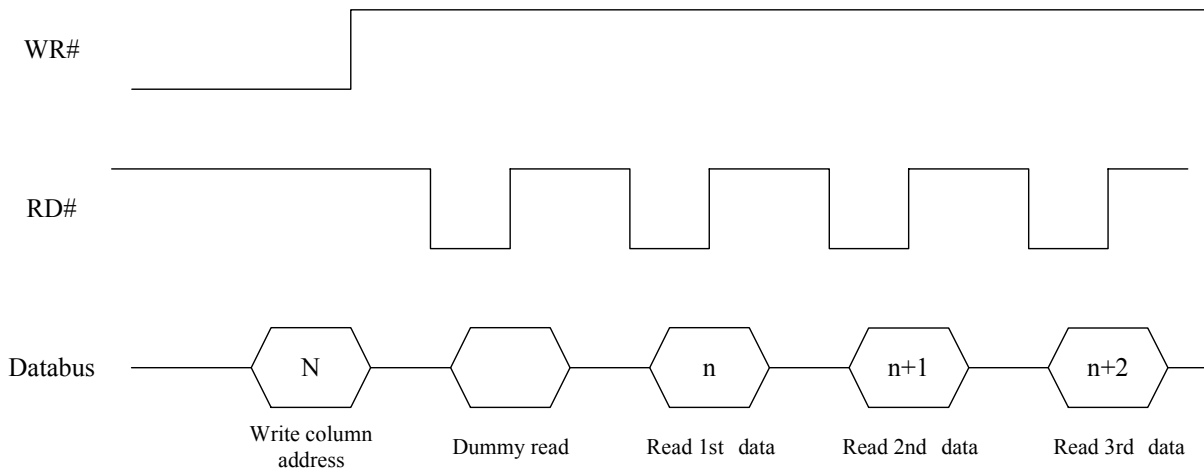
Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# (WR#)# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

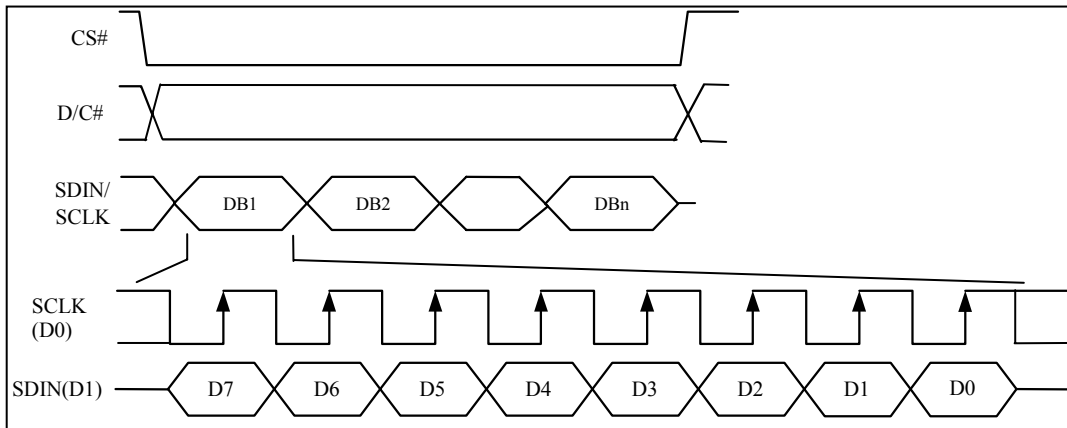
Note

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal
- (3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

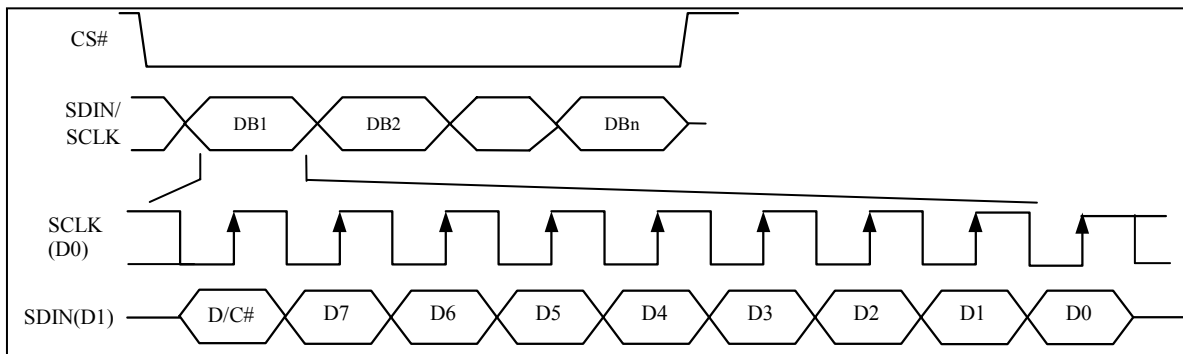
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Under serial mode, only write operations are allowed.

Table 8-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0	Note
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑	(1) L stands for LOW in signal
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑	(2) ↑ stands for rising edge of signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D₂ for output and SDA_{IN}/D₁ for input) and I²C-bus clock signal SCL (D₀). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)

SSD1309 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b₇ b₆ b₅ b₄ b₃ b₂ b₁ b₀
0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1309. D/C# pin acts as SA0 for slave address selection.

“R/W#” bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)

SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

“SDA_{IN}” and “SDA_{OUT}” are tied together and serve as SDA. The “SDA_{IN}” pin must be connected to act as SDA. The “SDA_{OUT}” pin may be disconnected. When “SDA_{OUT}” pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

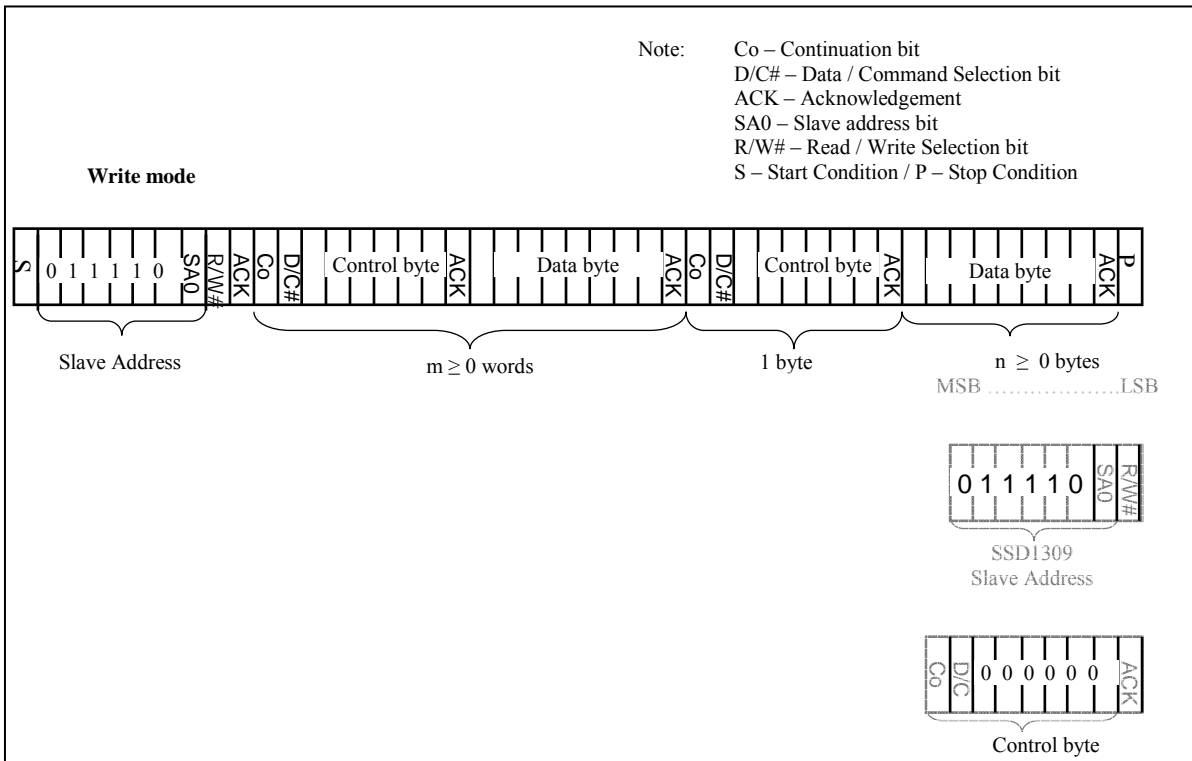
c) I²C-bus clock signal (SCL)

The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

8.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 8-7 for the write mode of I²C-bus in chronological order.

Figure 8-7 : I²C-bus data format



8.1.5.2 Write mode for I²C

- 1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
- 2) The slave address is following the start condition for recognition use. For the SSD1309, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
- 3) The write mode is established by setting the R/W# bit to logic “0”.
- 4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
- 5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
 - a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
 - b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
- 6) Acknowledge bit will be generated after receiving each control byte or data byte.
- 7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 8-8 : Definition of the Start and Stop Condition

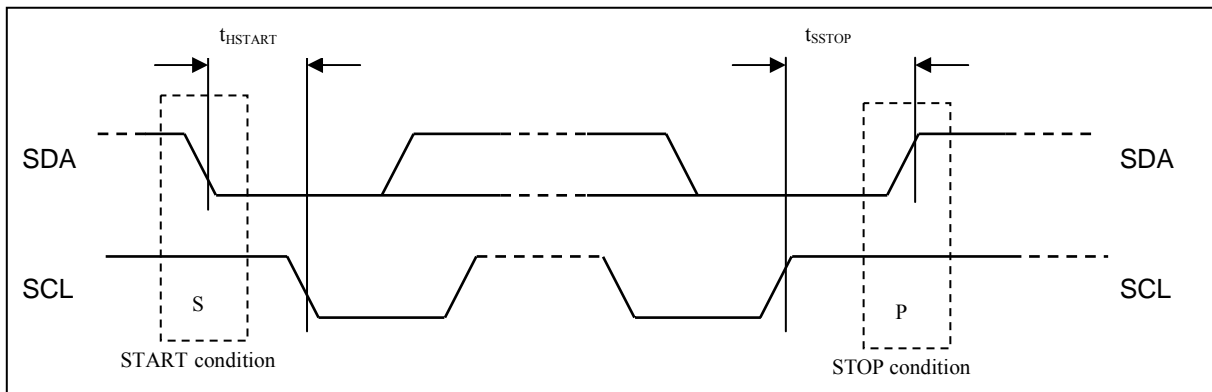
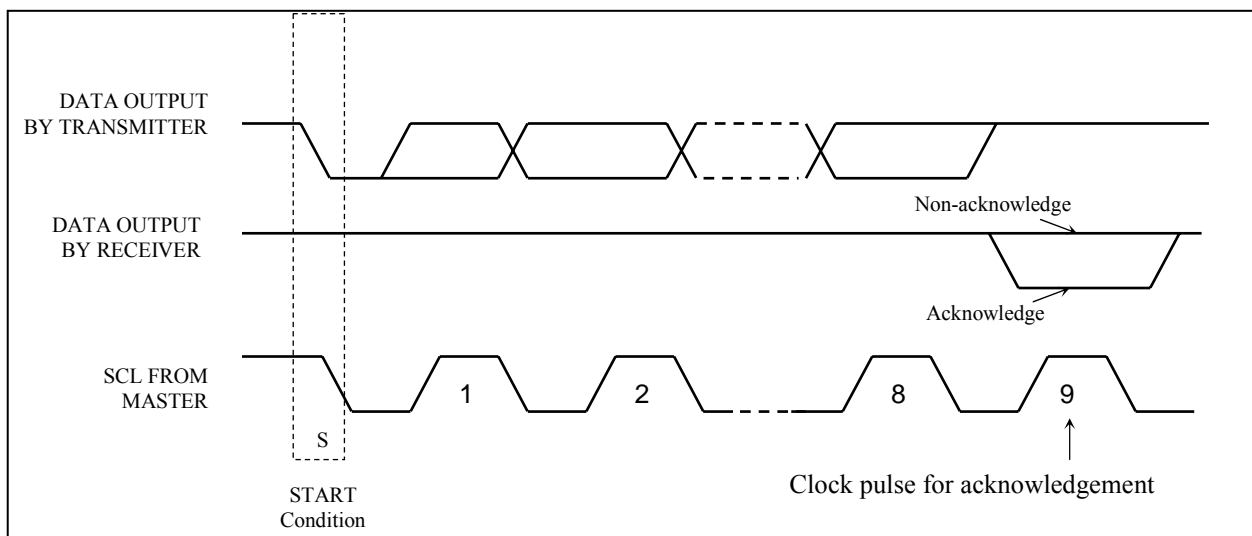


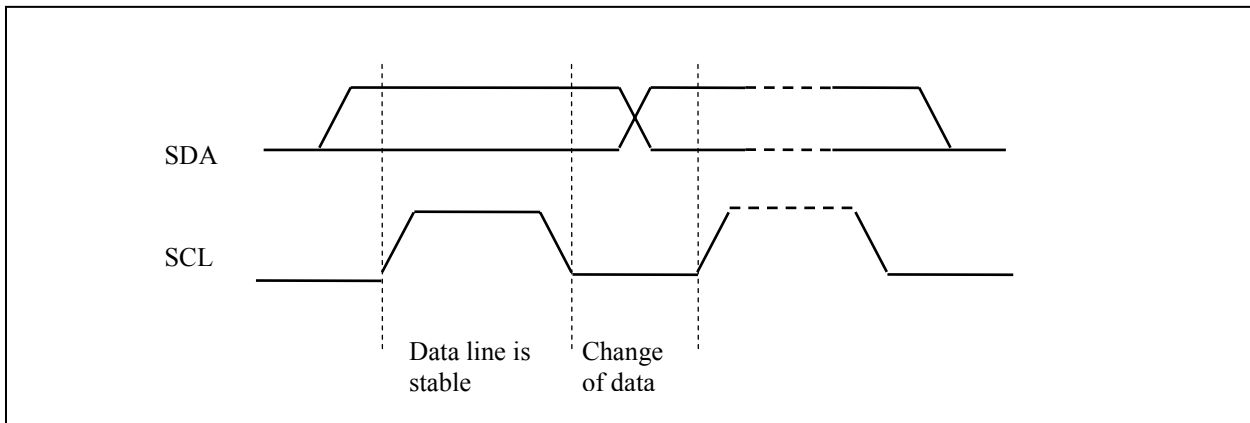
Figure 8-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 8-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 8-10 : Definition of the data transfer condition



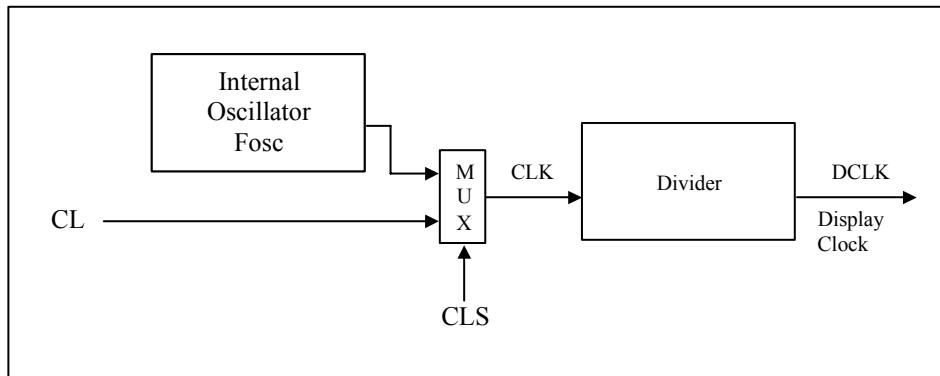
8.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{osc} can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + K_o$
 $= 2 + 2 + 65 = 69$ at power on reset (that is K_o is a constant that equals to 65)
 (Please refer to Section 8.5 “Segment Drivers / Common Drivers” for the details of the “Phase”)
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

8.4 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

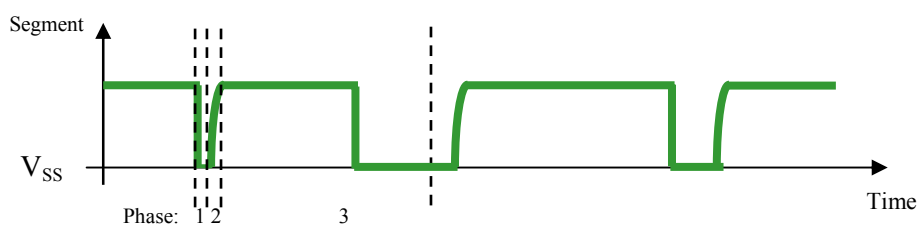
8.5 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted from 0 to 320uA with 256 steps. Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from V_{SS} . The period of phase 2 can be programmed in length from 1 to 15 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 8-12 : Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 65, after finishing 65 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

8.6 Graphic Display Data RAM (GDDRAM)

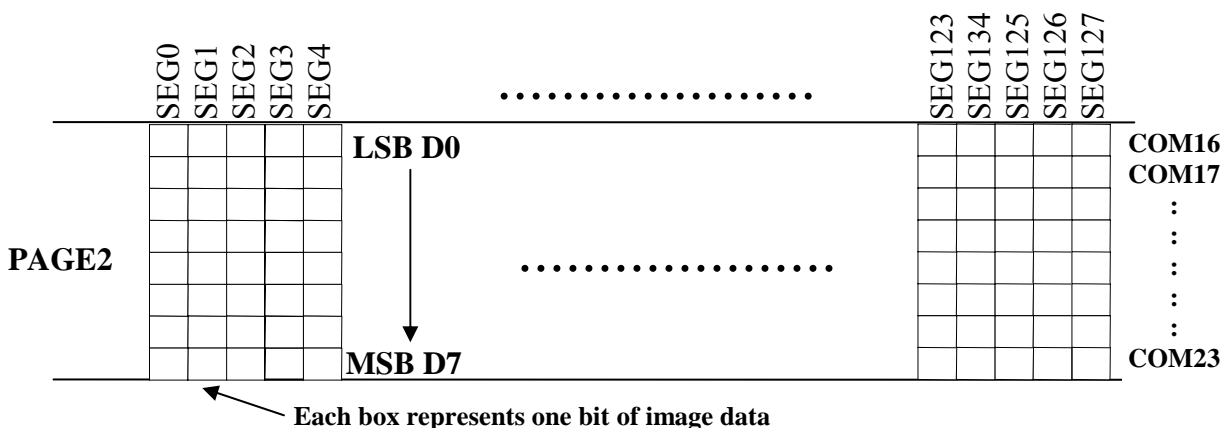
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Figure 8-13 : GDDRAM pages structure of SSD1309

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48-COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 -----SEG127	
Column re-mapping	SEG127 -----SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in Figure 8-14.

Figure 8-14 : Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in Figure 8-13.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

8.7 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

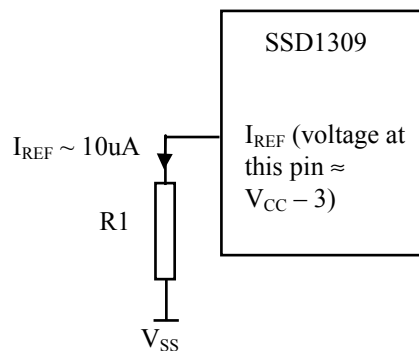
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = (\text{Contrast}+1) / 8 \times I_{REF}$$

in which the contrast (0~255) is set by Set Contrast command 81h

The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 8-15. It is recommended to set I_{REF} to $10 \pm 2\mu\text{A}$ so as to achieve $I_{SEG} = 320\mu\text{A}$ at maximum contrast 255.

Figure 8-15 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 3\text{V}$, the value of resistor $R1$ can be found as below:

For $I_{REF} = 10\mu\text{A}$, $V_{CC} = 12\text{V}$:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &\approx (12 - 3) / 10\mu\text{A} \\ &= 900\text{k}\Omega \end{aligned}$$

