SSD1329

Advance Information

128 x 128 OLED Segment / Common Driver with Controller Equips with 16 Gray Scale Levels and 64 Hard Icon Lines

Appendix: IC Revision history of SSD1329 Specification

Version	Change Items	Effective Date
1.0	1st Release	23-Dec-05
1.1	1. Revised Figure 5-1: SSD1329Z Die Drawing (rotate orientation) 2. Updated Section 2 Features 3. Updated command table and command description of command 4. Revised Table 13-1	6-Jan-06
1.2	1. Revised content in DC Characteristics 2. Revised content in AC Characteristics 3. Revised content in Maximum Ratings 4. Added horizontal and vertical scrolling along with all other graphic commands 5. Added Section 8.11 Power ON and OFF Sequence	06-Mar-06
1.3	1. Revise section 8.1, 8.1.2 & Section 13 (8080 interface) 2. Update Section 8.11 Power On / OFF sequence 3. Modify Section 8.1.3 MCU Serial Interface 4. Revise command table	11-Aug-06
1.4	1. Clarify pulse width definition in Section 8.2 Segment Drivers/Common Drivers 2. Clarify command B1h, B2h, B7h, B8h	09-Oct-06
1.5	1. Revise typo : phase1, phase2 DCLK range from 1~16 to 1~15 in 8.2 2. Revise command description of command 81h	10-Jan-07
1.6	1. Add China RoHS disclaimer at the last page. 2. Revise VCC range in a. Table 11-1 VCC Maximum Ratings: from 0 to +18.0 change to 0 to +19.0 b. Table 12-1 Max VCC from 16V change to 18V 3. Add light sensitive note In Section 11 – Maximum rating	02-May-07
1.7	1. Updated Section 3 Ordering information 2. Updated the die size info (after sawing) in Section 5 3. Updated and added notes in Section 8.11 Power ON OFF sequence	07-May-09
1.8	1. P.9 Revise bump size typo 2. P.66 Revise disclaimer	17-Mar-11

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TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1329 is a single-chip CMOS OLED/PLED driver with controller for 16 gray scale levels organic / polymer light emitting diode dot-matrix graphic display system. SSD1329 consists of 128 segments, 128 commons and 64 hard icons. This IC is designed for Common Cathode type OLED / PLED panel.

SSD1329 displays data directly from its internal 128 x 128 x 4 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Support maximum of 128 x 128 matrix panel
- Support 64 hard icons, 2 icon rows with 2 pins for each row
- Power supply: V_{DD} = 2.4V ~ 3.5V
  V_{CI} = 3.2V ~ 4.2V
  V_{DDIO} = 1.7V ~ V_{DD}
  V_{CC} = 9.0V ~ 18.0V
- For matrix display:
  - Can output maximum segment source current: 350uA
  - Common maximum sink current: 40mA
- For hard icons:
  - Segment maximum source current: 127.5uA
  - 128 steps current control
- DC-DC 2X voltage converter for hard icons
- Embedded 128 x 128 x 4 bit SRAM display buffer
- 256 steps contrast current control
- Internal oscillator
- Programmable frame rate
- 8-bit 6800-series Parallel Interface, 8080-series Parallel Interface and Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 85 °C

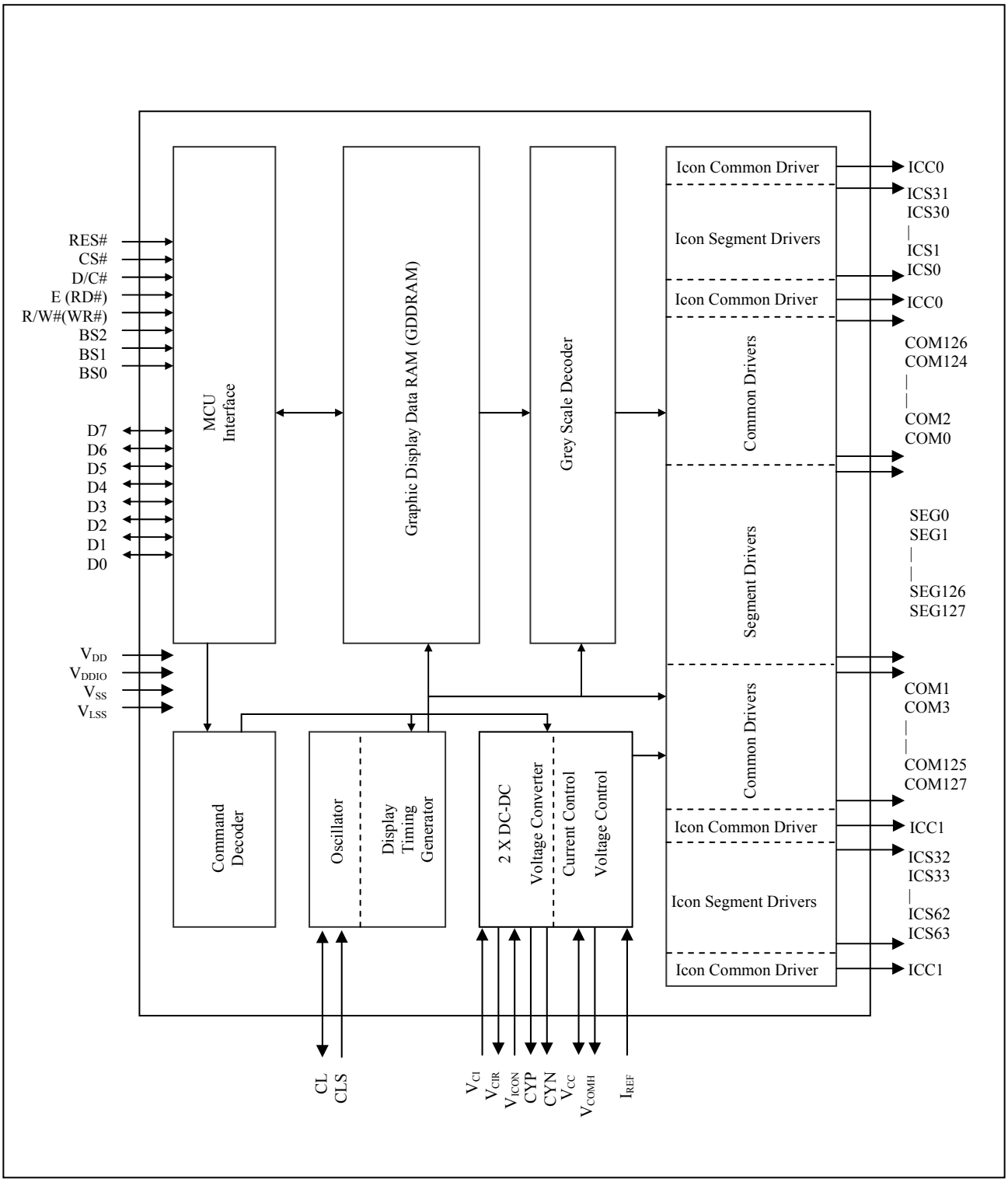
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Icon SEG	Icon COM	Package Form	Reference	Remark
SSD1329Z	128	128	64	2	COG	Page 9	• Min SEG pad pitch: 43.2 um • Min COM pad pitch: 51.8 um
SSD1329T1R1	128	128	48	2	TAB	Page 13, 64	• 8-bit 80 / 68 / SPI interface • Output lead pitch: 0.049925mm • 5 SPH, 35m film

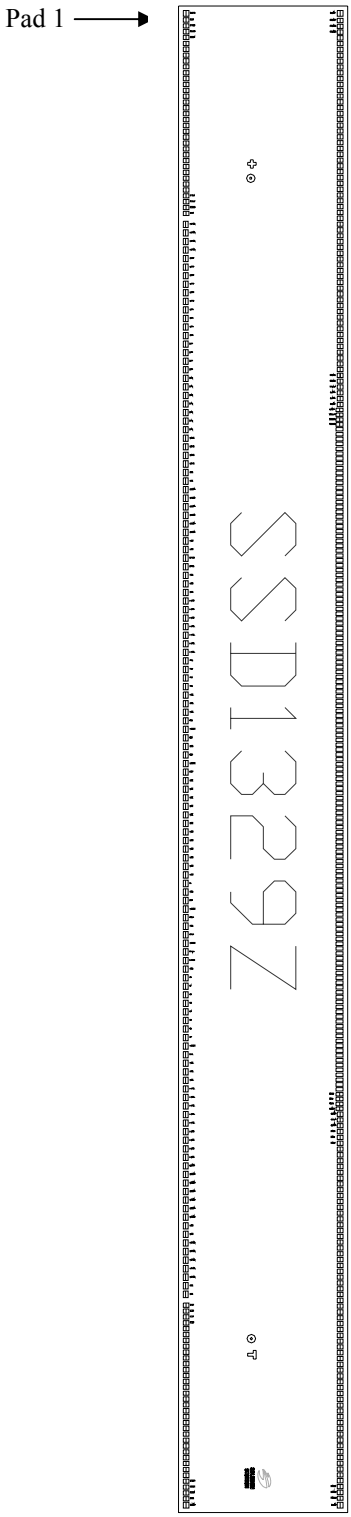
4 BLOCK DIAGRAM

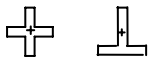
Figure 4-1: SSD1329 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1329Z Die Drawing





Note

[1] + represents the center of the alignment mark

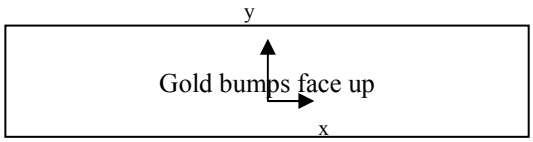
	X-Axis (um)	Y-Axis (um)
	+5300.0	-100.0
	-5300.0	-100.0

All alignment keys have size 75 um x 75 um

Die Size (after sawing)	13410 ±50 um x 1504 ±50 um
Die Thickness	457 um ± 25 um
Min I/O pad pitch	76.2 um
Min SEG pad pitch	43.2 um
Min COM pad pitch	51.8 um
Bump Height	Nominal 15 um

Bump Size

Pad #	**X [um]**	**Y [um]**
1, 196, 197, 477	50	52
2-35, 162-195	37.2	52
36-161	56	44
198-264, 410-476	36.8	52
265-409	28.2	64



Pad 1,2,3 …→

Figure 5-2: SSD1329Z Alignment Mark Dimensions

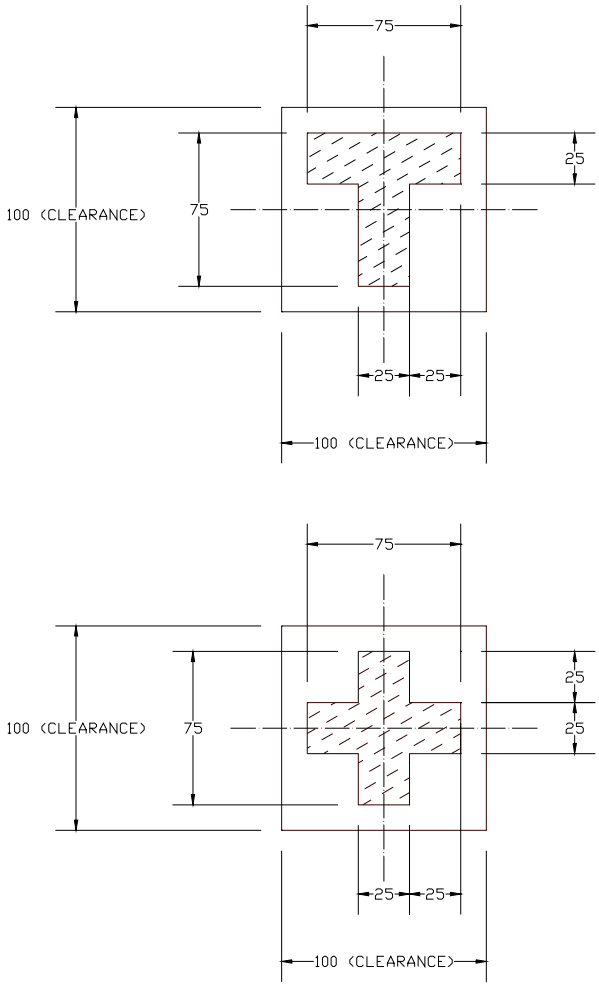


Table 5-1: SSD1329Z Bump Die Pad Coordinates

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
1	DUMMY	-6640.0	-686.0	81	VLSS	-1333.5	-690.0	161	VCC	4762.5	-690.0	241	COM20	4349.8	686.0
2	ICC1	-6582.0	-686.0	82	VLSS	-1257.3	-690.0	162	ICC0	4859.4	-686.0	242	COM19	4298.0	686.0
3	ICS32	-6529.8	-686.0	83	VLSS	-1181.1	-690.0	163	ICS0	4911.6	-686.0	243	COM18	4246.2	686.0
4	ICS33	-6477.6	-686.0	84	VLSS	-1104.9	-690.0	164	ICS1	4963.8	-686.0	244	COM17	4194.4	686.0
5	ICS34	-6425.4	-686.0	85	VLSS	-1028.7	-690.0	165	ICS2	5016.0	-686.0	245	COM16	4142.6	686.0
6	ICS35	-6373.2	-686.0	86	VLSS	-952.5	-690.0	166	ICS3	5068.2	-686.0	246	COM15	4090.8	686.0
7	ICS36	-6321.0	-686.0	87	TR3	-876.3	-690.0	167	ICS4	5120.4	-686.0	247	COM14	4039.0	686.0
8	ICS37	-6268.8	-686.0	88	TR2	-800.1	-690.0	168	ICS5	5172.6	-686.0	248	COM13	3987.2	686.0
9	ICS38	-6216.6	-686.0	89	TR1	-723.9	-690.0	169	ICS6	5224.8	-686.0	249	COM12	3935.4	686.0
10	ICS39	-6164.4	-686.0	90	TR0	-647.7	-690.0	170	ICS7	5277.0	-686.0	250	COM11	3883.6	686.0
11	ICS40	-6112.2	-686.0	91	VSS	-571.5	-690.0	171	ICS8	5329.2	-686.0	251	COM10	3831.8	686.0
12	ICS41	-6060.0	-686.0	92	VSS	-495.3	-690.0	172	ICS9	5381.4	-686.0	252	COM9	3780.0	686.0
13	ICS42	-6007.8	-686.0	93	VSS	-419.1	-690.0	173	ICS10	5433.6	-686.0	253	COM8	3728.2	686.0
14	ICS43	-5955.6	-686.0	94	BS0	-342.9	-690.0	174	ICS11	5485.8	-686.0	254	COM7	3676.4	686.0
15	ICS44	-5903.4	-686.0	95	VDDIO	-266.7	-690.0	175	ICS12	5538.0	-686.0	255	COM6	3624.6	686.0
16	ICS45	-5851.2	-686.0	96	BS1	-190.5	-690.0	176	ICS13	5590.2	-686.0	256	COM5	3572.8	686.0
17	ICS46	-5799.0	-686.0	97	VSS	-114.3	-690.0	177	ICS14	5642.4	-686.0	257	COM4	3521.0	686.0
18	ICS47	-5746.8	-686.0	98	BS2	-38.1	-690.0	178	ICS15	5694.6	-686.0	258	COM3	3469.2	686.0
19	ICS48	-5694.6	-686.0	99	VDDIO	38.1	-690.0	179	ICS16	5746.8	-686.0	259	COM2	3417.4	686.0
20	ICS49	-5642.4	-686.0	100	IREF	114.3	-690.0	180	ICS17	5799.0	-686.0	260	COM1	3365.6	686.0
21	ICS50	-5590.2	-686.0	101	VCC	190.5	-690.0	181	ICS18	5851.2	-686.0	261	COM0	3313.8	686.0
22	ICS51	-5538.0	-686.0	102	VCC	266.7	-690.0	182	ICS19	5903.4	-686.0	262	DUMMY	3262.0	686.0
23	ICS52	-5485.8	-686.0	103	VCC	342.9	-690.0	183	ICS20	5955.6	-686.0	263	DUMMY	3210.2	686.0
24	ICS53	-5433.6	-686.0	104	VCC	419.1	-690.0	184	ICS21	6007.8	-686.0	264	DUMMY	3158.4	686.0
25	ICS54	-5381.4	-686.0	105	VCC	495.3	-690.0	185	ICS22	6060.0	-686.0	265	DUMMY	3110.4	680.0
26	ICS55	-5329.2	-686.0	106	VCC	571.5	-690.0	186	ICS23	6112.2	-686.0	266	SEG0	3067.2	680.0
27	ICS56	-5277.0	-686.0	107	VDD	647.7	-690.0	187	ICS24	6164.4	-686.0	267	SEG1	3024.0	680.0
28	ICS57	-5224.8	-686.0	108	VDD	723.9	-690.0	188	ICS25	6216.6	-686.0	268	SEG2	2980.8	680.0
29	ICS58	-5172.6	-686.0	109	VDD	800.1	-690.0	189	ICS26	6268.8	-686.0	269	SEG3	2937.6	680.0
30	ICS59	-5120.4	-686.0	110	VDD	876.3	-690.0	190	ICS27	6321.0	-686.0	270	SEG4	2894.4	680.0
31	ICS60	-5068.2	-686.0	111	VDD	952.5	-690.0	191	ICS28	6373.2	-686.0	271	SEG5	2851.2	680.0
32	ICS61	-5016.0	-686.0	112	VDD	1028.7	-690.0	192	ICS29	6425.4	-686.0	272	SEG6	2808.0	680.0
33	ICS62	-4963.8	-686.0	113	CL	1104.9	-690.0	193	ICS30	6477.6	-686.0	273	SEG7	2764.8	680.0
34	ICS63	-4911.6	-686.0	114	VSS	1181.1	-690.0	194	ICS31	6529.8	-686.0	274	SEG8	2721.6	680.0
35	ICC1	-4859.4	-686.0	115	CS#	1257.3	-690.0	195	ICC0	6582.0	-686.0	275	SEG9	2678.4	680.0
36	VICON	-4762.5	-690.0	116	VDDIO	1333.5	-690.0	196	DUMMY	6640.0	-686.0	276	SEG10	2635.2	680.0
37	VICON	-4686.3	-690.0	117	RES#	1409.7	-690.0	197	DUMMY	6640.0	686.0	277	SEG11	2592.0	680.0
38	VICON	-4610.1	-690.0	118	VSS	1485.9	-690.0	198	COM63	6577.2	686.0	278	SEG12	2548.8	680.0
39	VICON	-4533.9	-690.0	119	D/C#	1562.1	-690.0	199	COM62	6525.4	686.0	279	SEG13	2505.6	680.0
40	VCIR	-4457.7	-690.0	120	VDDIO	1638.3	-690.0	200	COM61	6473.6	686.0	280	SEG14	2462.4	680.0
41	VCIR	-4381.5	-690.0	121	R/W#	1714.5	-690.0	201	COM60	6421.8	686.0	281	SEG15	2419.2	680.0
42	VCIR	-4305.3	-690.0	122	E/RD#	1790.7	-690.0	202	COM59	6370.0	686.0	282	SEG16	2376.0	680.0
43	VCIR	-4229.1	-690.0	123	VSS	1866.9	-690.0	203	COM58	6318.2	686.0	283	SEG17	2332.8	680.0
44	VCIR	-4152.9	-690.0	124	D0	1943.1	-690.0	204	COM57	6266.4	686.0	284	SEG18	2289.6	680.0
45	VCIR	-4076.7	-690.0	125	D1	2019.3	-690.0	205	COM56	6214.6	686.0	285	SEG19	2246.4	680.0
46	VCI1	-4000.5	-690.0	126	D2	2095.5	-690.0	206	COM55	6162.8	686.0	286	SEG20	2203.2	680.0
47	VCI1	-3924.3	-690.0	127	D3	2171.7	-690.0	207	COM54	6111.0	686.0	287	SEG21	2160.0	680.0
48	VCI1	-3848.1	-690.0	128	D4	2247.9	-690.0	208	COM53	6059.2	686.0	288	SEG22	2116.8	680.0
49	VCI1	-3771.9	-690.0	129	D5	2324.1	-690.0	209	COM52	6007.4	686.0	289	SEG23	2073.6	680.0
50	CYP	-3695.7	-690.0	130	D6	2400.3	-690.0	210	COM51	5955.6	686.0	290	SEG24	2030.4	680.0
51	CYP	-3619.5	-690.0	131	D7	2476.5	-690.0	211	COM50	5903.8	686.0	291	SEG25	1987.2	680.0
52	CYP	-3543.3	-690.0	132	VDDIO	2552.7	-690.0	212	COM49	5852.0	686.0	292	SEG26	1944.0	680.0
53	CYP	-3467.1	-690.0	133	CLS	2628.9	-690.0	213	COM48	5800.2	686.0	293	SEG27	1900.8	680.0
54	CYN	-3390.9	-690.0	134	VSS	2705.1	-690.0	214	COM47	5748.4	686.0	294	SEG28	1857.6	680.0
55	CYN	-3314.7	-690.0	135	VSS	2781.3	-690.0	215	COM46	5696.6	686.0	295	SEG29	1814.4	680.0
56	CYN	-3238.5	-690.0	136	VSS	2857.5	-690.0	216	COM45	5644.8	686.0	296	SEG30	1771.2	680.0
57	CYN	-3162.3	-690.0	137	VLSS	2933.7	-690.0	217	COM44	5593.0	686.0	297	SEG31	1728.0	680.0
58	CYN	-3086.1	-690.0	138	VLSS	3009.9	-690.0	218	COM43	5541.2	686.0	298	SEG32	1684.8	680.0
59	CYN	-3009.9	-690.0	139	VLSS	3086.1	-690.0	219	COM42	5489.4	686.0	299	SEG33	1641.6	680.0
60	CYN	-2933.7	-690.0	140	VLSS	3162.3	-690.0	220	COM41	5437.6	686.0	300	SEG34	1598.4	680.0
61	VCHS	-2857.5	-690.0	141	VLSS	3238.5	-690.0	221	COM40	5385.8	686.0	301	SEG35	1555.2	680.0
62	VCHS	-2781.3	-690.0	142	VLSS	3314.7	-690.0	222	COM39	5334.0	686.0	302	SEG36	1512.0	680.0
63	VCHS	-2705.1	-690.0	143	VLSS	3390.9	-690.0	223	COM38	5282.2	686.0	303	SEG37	1468.8	680.0
64	VCHS	-2628.9	-690.0	144	VLSS	3467.1	-690.0	224	COM37	5230.4	686.0	304	SEG38	1425.6	680.0
65	VCC	-2552.7	-690.0	145	VLSS	3543.3	-690.0	225	COM36	5178.6	686.0	305	SEG39	1382.4	680.0
66	VCC	-2476.5	-690.0	146	NC	3619.5	-690.0	226	COM35	5126.8	686.0	306	SEG40	1339.2	680.0
67	VCOMH	-2400.3	-690.0	147	VCOMH	3695.7	-690.0	227	COM34	5075.0	686.0	307	SEG41	1296.0	680.0
68	VCOMH	-2324.1	-690.0	148	VCOMH	3771.9	-690.0	228	COM33	5023.2	686.0	308	SEG42	1252.8	680.0
69	VCOMH	-2247.9	-690.0	149	VCOMH	3848.1	-690.0	229	COM32	4971.4	686.0	309	SEG43	1209.6	680.0
70	VCOMH	-2171.7	-690.0	150	VCOMH	3924.3	-690.0	230	COM31	4919.6	686.0	310	SEG44	1166.4	680.0
71	VCOMH	-2095.5	-690.0	151	VCOMH	4000.5	-690.0	231	COM30	4867.8	686.0	311	SEG45	1123.2	680.0
72	VCOMH	-2019.3	-690.0	152	VCOMH	4076.7	-690.0	232	COM29	4816.0	686.0	312	SEG46	1080.0	680.0
73	VDD	-1943.1	-690.0	153	VDD	4152.9	-690.0	233	COM28	4764.2	686.0	313	SEG47	1036.8	680.0
74	VDD	-1866.9	-690.0	154	VDD	4229.1	-690.0	234	COM27	4712.4	686.0	314	SEG48	993.6	680.0
75	GPIO0	-1790.7	-690.0	155	VICON	4305.3	-690.0	235	COM26	4660.6	686.0	315	SEG49	950.4	680.0
76	GPIO1	-1714.5	-690.0	156	VICON	4381.5	-690.0	236	COM25	4608.8	686.0	316	SEG50	907.2	680.0
77	VSS	-1638.3	-690.0	157	VICON	4457.7	-690.0	237	COM24	4557.0	686.0	317	SEG51	864.0	680.0
78	VSS	-1562.1	-690.0	158	VICON	4533.9	-690.0	238	COM23	4505.2	686.0	318	SEG52	820.8	680.0
79	VSS	-1485.9	-690.0	159	VICON	4610.1	-690.0	239	COM22	4453.4	686.0	319	SEG53	777.6	680.0
80	VLSS	-1409.7	-690.0	160	VCC	4686.3	-690.0	240	COM21	4401.6	686.0	320	SEG54	734.4	680.0

Pad #	Pad Name	X-Axis	Y-Axis
321	SEG55	691.2	680.0
322	SEG56	648.0	680.0
323	SEG57	604.8	680.0
324	SEG58	561.6	680.0
325	SEG59	518.4	680.0
326	DUMMY	475.2	680.0
327	DUMMY	432.0	680.0
328	DUMMY	388.8	680.0
329	DUMMY	345.6	680.0
330	DUMMY	302.4	680.0
331	DUMMY	259.2	680.0
332	DUMMY	216.0	680.0
333	DUMMY	172.8	680.0
334	DUMMY	129.6	680.0
335	DUMMY	86.4	680.0
336	DUMMY	43.2	680.0
337	DUMMY	0.0	680.0
338	DUMMY	-43.2	680.0
339	DUMMY	-86.4	680.0
340	DUMMY	-129.6	680.0
341	SEG60	-172.8	680.0
342	SEG61	-216.0	680.0
343	SEG62	-259.2	680.0
344	SEG63	-302.4	680.0
345	SEG64	-345.6	680.0
346	SEG65	-388.8	680.0
347	SEG66	-432.0	680.0
348	SEG67	-475.2	680.0
349	SEG68	-518.4	680.0
350	SEG69	-561.6	680.0
351	SEG70	-604.8	680.0
352	SEG71	-648.0	680.0
353	SEG72	-691.2	680.0
354	SEG73	-734.4	680.0
355	SEG74	-777.6	680.0
356	SEG75	-820.8	680.0
357	SEG76	-864.0	680.0
358	SEG77	-907.2	680.0
359	SEG78	-950.4	680.0
360	SEG79	-993.6	680.0
361	SEG80	-1036.8	680.0
362	SEG81	-1080.0	680.0
363	SEG82	-1123.2	680.0
364	SEG83	-1166.4	680.0
365	SEG84	-1209.6	680.0
366	SEG85	-1252.8	680.0
367	SEG86	-1296.0	680.0
368	SEG87	-1339.2	680.0
369	SEG88	-1382.4	680.0
370	SEG89	-1425.6	680.0
371	SEG90	-1468.8	680.0
372	SEG91	-1512.0	680.0
373	SEG92	-1555.2	680.0
374	SEG93	-1598.4	680.0
375	SEG94	-1641.6	680.0
376	SEG95	-1684.8	680.0
377	SEG96	-1728.0	680.0
378	SEG97	-1771.2	680.0
379	SEG98	-1814.4	680.0
380	SEG99	-1857.6	680.0
381	SEG100	-1900.8	680.0
382	SEG101	-1944.0	680.0
383	SEG102	-1987.2	680.0
384	SEG103	-2030.4	680.0
385	SEG104	-2073.6	680.0
386	SEG105	-2116.8	680.0
387	SEG106	-2160.0	680.0
388	SEG107	-2203.2	680.0
389	SEG108	-2246.4	680.0
390	SEG109	-2289.6	680.0
391	SEG110	-2332.8	680.0
392	SEG111	-2376.0	680.0
393	SEG112	-2419.2	680.0
394	SEG113	-2462.4	680.0
395	SEG114	-2505.6	680.0
396	SEG115	-2548.8	680.0
397	SEG116	-2592.0	680.0
398	SEG117	-2635.2	680.0
399	SEG118	-2678.4	680.0
400	SEG119	-2721.6	680.0

Pad #	Pad Name	X-Axis	Y-Axis
401	SEG120	-2764.8	680.0
402	SEG121	-2808.0	680.0
403	SEG122	-2851.2	680.0
404	SEG123	-2894.4	680.0
405	SEG124	-2937.6	680.0
406	SEG125	-2980.8	680.0
407	SEG126	-3024.0	680.0
408	SEG127	-3067.2	680.0
409	DUMMY	-3110.4	680.0
410	DUMMY	-3158.4	686.0
411	DUMMY	-3210.2	686.0
412	DUMMY	-3262.0	686.0
413	COM64	-3313.8	686.0
414	COM65	-3365.6	686.0
415	COM66	-3417.4	686.0
416	COM67	-3469.2	686.0
417	COM68	-3521.0	686.0
418	COM69	-3572.8	686.0
419	COM70	-3624.6	686.0
420	COM71	-3676.4	686.0
421	COM72	-3728.2	686.0
422	COM73	-3780.0	686.0
423	COM74	-3831.8	686.0
424	COM75	-3883.6	686.0
425	COM76	-3935.4	686.0
426	COM77	-3987.2	686.0
427	COM78	-4039.0	686.0
428	COM79	-4090.8	686.0
429	COM80	-4142.6	686.0
430	COM81	-4194.4	686.0
431	COM82	-4246.2	686.0
432	COM83	-4298.0	686.0
433	COM84	-4349.8	686.0
434	COM85	-4401.6	686.0
435	COM86	-4453.4	686.0
436	COM87	-4505.2	686.0
437	COM88	-4557.0	686.0
438	COM89	-4608.8	686.0
439	COM90	-4660.6	686.0
440	COM91	-4712.4	686.0
441	COM92	-4764.2	686.0
442	COM93	-4816.0	686.0
443	COM94	-4867.8	686.0
444	COM95	-4919.6	686.0
445	COM96	-4971.4	686.0
446	COM97	-5023.2	686.0
447	COM98	-5075.0	686.0
448	COM99	-5126.8	686.0
449	COM100	-5178.6	686.0
450	COM101	-5230.4	686.0
451	COM102	-5282.2	686.0
452	COM103	-5334.0	686.0
453	COM104	-5385.8	686.0
454	COM105	-5437.6	686.0
455	COM106	-5489.4	686.0
456	COM107	-5541.2	686.0
457	COM108	-5593.0	686.0
458	COM109	-5644.8	686.0
459	COM110	-5696.6	686.0
460	COM111	-5748.4	686.0
461	COM112	-5800.2	686.0
462	COM113	-5852.0	686.0
463	COM114	-5903.8	686.0
464	COM115	-5955.6	686.0
465	COM116	-6007.4	686.0
466	COM117	-6059.2	686.0
467	COM118	-6111.0	686.0
468	COM119	-6162.8	686.0
469	COM120	-6214.6	686.0
470	COM121	-6266.4	686.0
471	COM122	-6318.2	686.0
472	COM123	-6370.0	686.0
473	COM124	-6421.8	686.0
474	COM125	-6473.6	686.0
475	COM126	-6525.4	686.0
476	COM127	-6577.2	686.0
477	DUMMY	-6640.0	686.0

6 PIN ARRANGEMENT

6.1 SSD1329T1R1 pin assignment

Figure 6-1: SSD1329T1R1 Pin Assignment

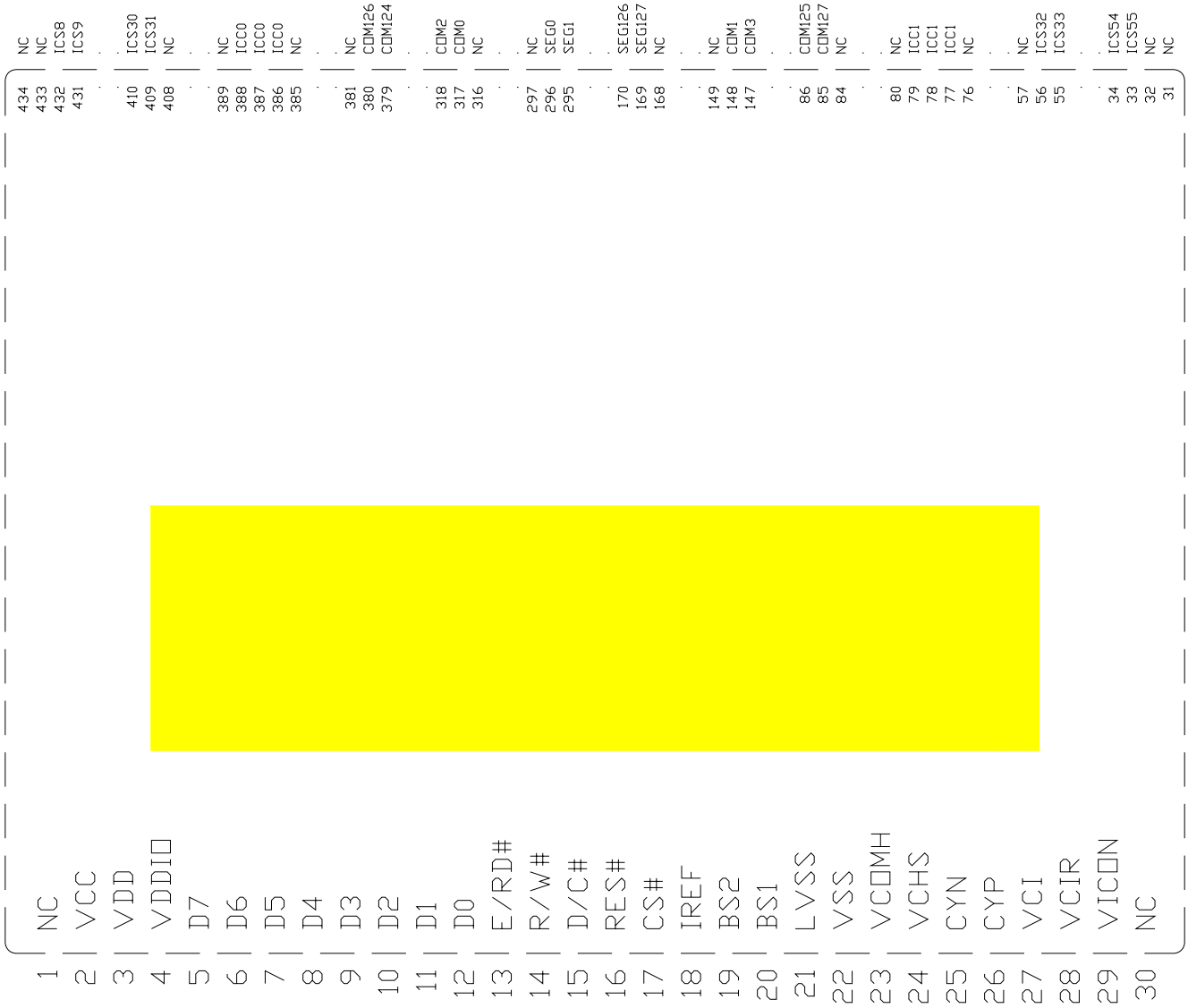


Table 6-1: SSD1329T1R1 Pin Assignment Table

Pad no	Pad Name
1	NC
2	VCC
3	VDD
4	VDDIO
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E/RD#
14	R/W#
15	D/C#
16	RES#
17	CS#
18	IREF
19	BS2
20	BS1
21	LVSS
22	VSS
23	VCOMH
24	VCHS
25	CYN
26	CYP
27	VCI
28	VCIR
29	VICON
30	NC
31	NC
32	NC
33	IC55
34	IC54
35	IC53
36	IC52
37	IC51
38	IC50
39	IC49
40	IC48
41	IC47
42	IC46
43	IC45
44	IC44
45	IC43
46	IC42
47	IC41
48	IC40
49	IC39
50	IC38
51	IC37
52	IC36
53	IC35
54	IC34
55	IC33
56	IC32
57	NC
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	NC
75	NC
76	NC
77	ICC1
78	ICC1
79	ICC1
80	NC
81	NC
82	NC
83	NC
84	NC
85	COM127
86	COM125
87	COM123
88	COM121
89	COM119
90	COM117
91	COM115
92	COM113
93	COM111
94	COM109
95	COM107
96	COM105
97	COM103
98	COM101
99	COM99
100	COM97
101	COM95
102	COM93
103	COM91
104	COM89
105	COM87
106	COM85
107	COM83
108	COM81
109	COM79
110	COM77
111	COM75
112	COM73
113	COM71
114	COM69
115	COM67
116	COM65
117	COM63
118	COM61
119	COM59
120	COM57
121	COM55
122	COM53
123	COM51
124	COM49
125	COM47
126	COM45
127	COM43
128	COM41
129	COM39
130	COM37
131	COM35
132	COM33
133	COM31
134	COM29
135	COM27
136	COM25
137	COM23
138	COM21
139	COM19
140	COM17
141	COM15
142	COM13
143	COM11
144	COM9
145	COM7
146	COM5
147	COM3
148	COM1
149	NC
150	NC
151	NC
152	NC
153	NC
154	NC
155	NC
156	NC
157	NC
158	NC
159	NC
160	NC
161	NC
162	NC
163	NC
164	NC
165	NC
166	NC
167	NC
168	NC
169	SEG127
170	SEG126
171	SEG125
172	SEG124
173	SEG123
174	SEG122
175	SEG121
176	SEG120
177	SEG119
178	SEG118
179	SEG117
180	SEG116
181	SEG115
182	SEG114
183	SEG113
184	SEG112
185	SEG111
186	SEG110
187	SEG109
188	SEG108
189	SEG107
190	SEG106
191	SEG105
192	SEG104
193	SEG103
194	SEG102
195	SEG101
196	SEG100
197	SEG99
198	SEG98
199	SEG97
200	SEG96
201	SEG95
202	SEG94
203	SEG93
204	SEG92
205	SEG91
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213	SEG83
214	SEG82
215	SEG81
216	SEG80
217	SEG79
218	SEG78
219	SEG77
220	SEG76
221	SEG75
222	SEG74
223	SEG73
224	SEG72
225	SEG71
226	SEG70
227	SEG69
228	SEG68
229	SEG67
230	SEG66
231	SEG65
232	SEG64
233	SEG63
234	SEG62
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247	SEG49
248	SEG48
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250	SEG46
251	SEG45
252	SEG44
253	SEG43
254	SEG42
255	SEG41
256	SEG40
257	SEG39
258	SEG38
259	SEG37
260	SEG36
261	SEG35
262	SEG34
263	SEG33
264	SEG32
265	SEG31
266	SEG30
267	SEG29
268	SEG28
269	SEG27
270	SEG26
271	SEG25
272	SEG24
273	SEG23
274	SEG22
275	SEG21
276	SEG20
277	SEG19
278	SEG18
279	SEG17
280	SEG16
281	SEG15
282	SEG14
283	SEG13
284	SEG12
285	SEG11
286	SEG10
287	SEG9
288	SEG8
289	SEG7
290	SEG6
291	SEG5
292	SEG4
293	SEG3
294	SEG2
295	SEG1
296	SEG0
297	NC
298	NC
299	NC
300	NC
301	NC
302	NC
303	NC
304	NC
305	NC
306	NC
307	NC
308	NC
309	NC
310	NC
311	NC
312	NC
313	NC
314	NC
315	NC
316	NC
317	COM0
318	COM2
319	COM4
320	COM6
321	COM8
322	COM10
323	COM12
324	COM14
325	COM16
326	COM18
327	COM20
328	COM22
329	COM24
330	COM26
331	COM28
332	COM30
333	COM32
334	COM34
335	COM36
336	COM38
337	COM40
338	COM42
339	COM44
340	COM46
341	COM48
342	COM50
343	COM52
344	COM54
345	COM56
346	COM58
347	COM60
348	COM62
349	COM64
350	COM66
351	COM68
352	COM70
353	COM72
354	COM74
355	COM76
356	COM78
357	COM80
358	COM82
359	COM84
360	COM86
361	COM88
362	COM90
363	COM92
364	COM94
365	COM96
366	COM98
367	COM100
368	COM102
369	COM104
370	COM106
371	COM108
372	COM110
373	COM112
374	COM114
375	COM116
376	COM118
377	COM120
378	COM122
379	COM124
380	COM126
381	NC
382	NC
383	NC
384	NC
385	NC
386	ICC0
387	ICC0
388	ICC0
389	NC
390	NC
391	NC
392	NC
393	NC
394	NC
395	NC
396	NC
397	NC
398	NC
399	NC
400	NC
401	NC
402	NC
403	NC
404	NC
405	NC
406	NC
407	NC
408	NC
409	ICS31
410	ICS30
411	ICS29
412	ICS28
413	ICS27
414	ICS26
415	ICS25
416	ICS24
417	ICS23
418	ICS22
419	ICS21
420	ICS20
421	ICS19
422	ICS18
423	ICS17
424	ICS16
425	ICS15
426	ICS14
427	ICS13
428	ICS12
429	ICS11
430	ICS10
431	ICS9
432	ICS8
433	NC
434	NC

7 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin

Table 7-1: Pin Descriptions

Pin Name	Pin Type	Description
RES#	I	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DDIO}) during normal operation.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled LOW.
D/C#	I	This pin is Data/Command control pin. When the pin is pulled HIGH (i.e. connect to V_{DDIO}), the data at D[7:0] is treated as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams in Figure 13-1 to Figure 13-4.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to V_{DDIO}) and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the chip is selected.
R/W# (WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DDIO}) and write mode will be carried out when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
D[7:0]	IO	These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.
BS[2:0]	I	These pins are MCU bus interface selection. Please refer to Table 7-2 for detail selection.
V_{DDIO}	P	This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have voltage high reference to V_{DDIO}. When I/O signal pins (BS0, BS1, BS2, CLS, CL, D[7:0], interface signals…) pull HIGH, they should be connected to V_{DDIO}.
V_{DD}	P	This pin in power supply for low volt logic. It must be connected to external source.
$V_{SS,}$ V_{LSS}	P	These pins are ground pin and also act as ground reference for the logic pins. They must be connected to external ground.
CL	IO	This pin is the system clock input. When internal oscillator is disabled (i.e. CLS is pulled LOW), this pin receives display clock signal from external clock source. When internal clock is enabled (i.e. CLS is pulled HIGH), this pin should be left open and nothing should be connected to this pin.
CLS	I	This is the internal clock enable pin. When this pin is pulled HIGH (i.e. connect to V_{DDIO}), internal oscillator is selected. The internal clock will be disabled when it is pulled LOW, an external clock source must be connected to CL pin for normal operation.

Pin Name	Pin Type	Description
V_{CC}	P	This pin is the most positive voltage supply of the chip. It is supplied either by external high voltage source or internal booster.
V_{COMH}	P	A capacitor should be connected between this pin and V_{SS}. No external power supply is allowed to connect to this pin.
I_{REF}	I	This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF}. A resistor should be connected between this pin and V_{DD} to maintain the current around 10uA.
COM0 ~ COM127	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is OFF.
ICS0 ~ ICS63	O	These pins provide the Segment driving signals for hard icons.
ICC0 ~ ICC1	O	These pins provide the Common driving signals for hard icons.
V_{CI}	P	This is the power supply pin of hard icon DC-DC voltage converter. It must be supplied externally when in-used. When hard icon DC-DC converter is not used, this pin should be left floated.
V_{ICON}	P	This is the power output pin for DC-DC converter to drive hard icons. A 2uF capacitor is recommended to connect from this pin to the ground. If internal DC-DC converter is disabled, this pin is acted as the power input pin for driving hard icons externally.
V_{CHS}	P	This is the ground pin for hard icon DC-DC voltage converter. It must be connected to external ground.
CYP, CYN	O	When the hard icon DC-DC voltage converter is used, a capacitor should be connected in between these pins. The recommended value of this capacitor is 1uF.
V_{CIR}	O	When the hard icon DC-DC voltage converter is in-used, a resistor should be connected between V_{CI} and this pin. The recommended value of this resistor is 20Ω. When hard icon DC-DC converter is not used, this pin should be left floated.

Table 7-2: MCU Bus Interface Pin Selection

Pin Name	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MPU Interface selection

SSD1329 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 7-2 for BS[2:0] setting).

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

8.1.1 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

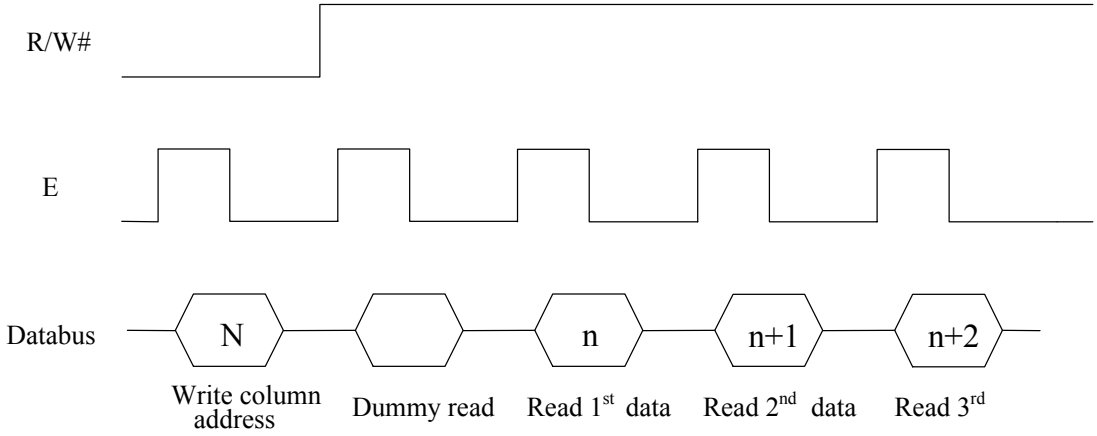
Table 8-2: Control pins of 6800 interface

Function	**E**	**R/W#**	**CS#**	**D/C#**
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1: Data read back procedure - insertion of dummy read



8.1.2 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

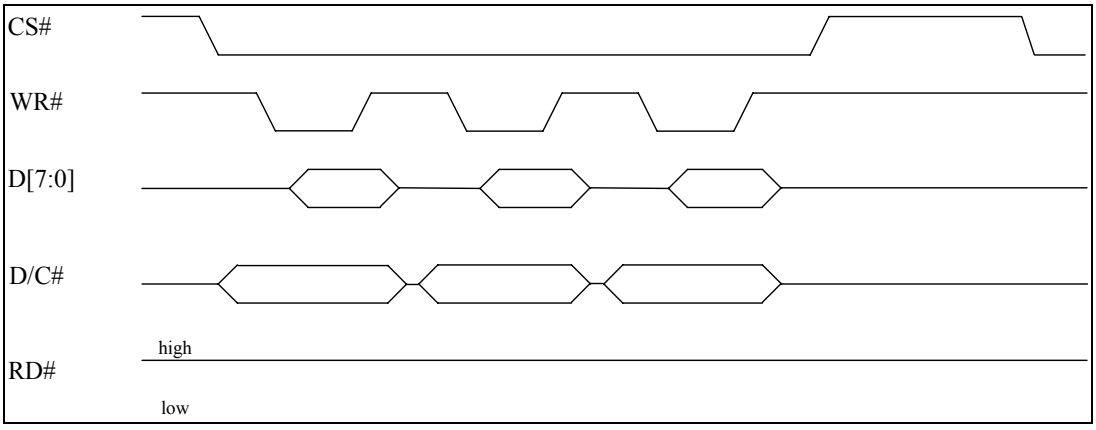


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

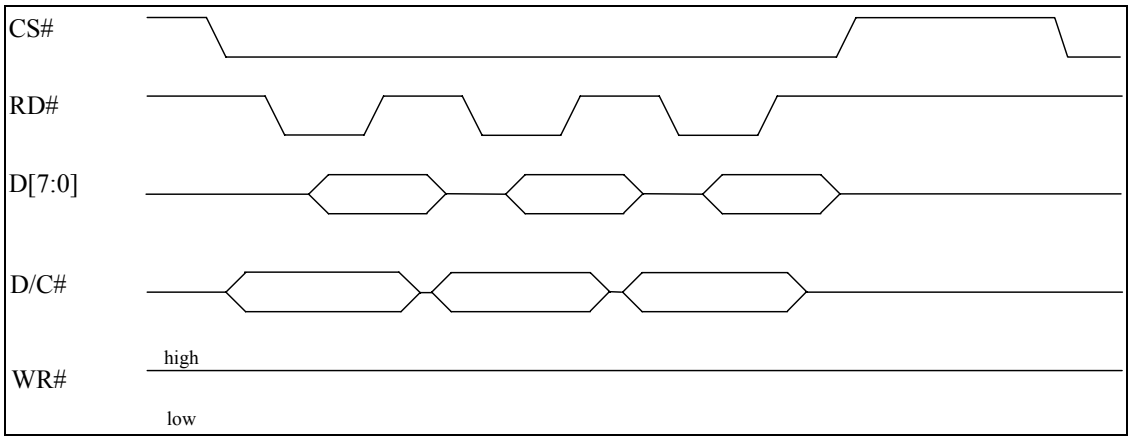


Table 8-3: Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

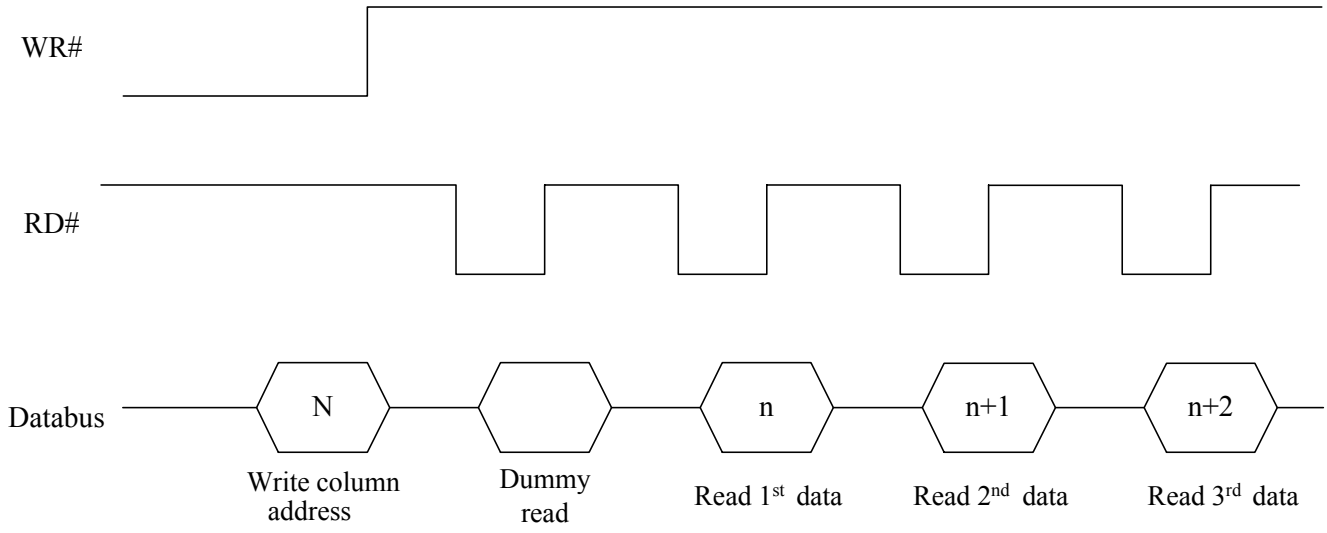
Table 8-4: Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 8-2 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4: Display data read back procedure - insertion of dummy read



8.1.3 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

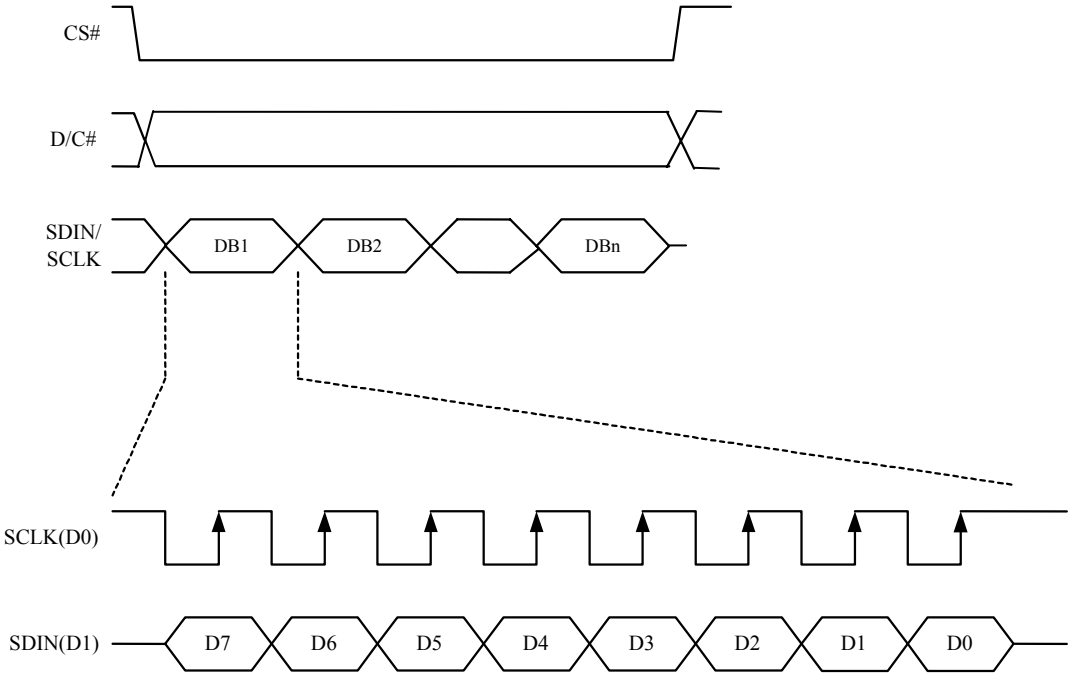
Table 8-5: Control pins of Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	Tie LOW	L	L
Write data	Tie LOW	Tie LOW	L	H

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

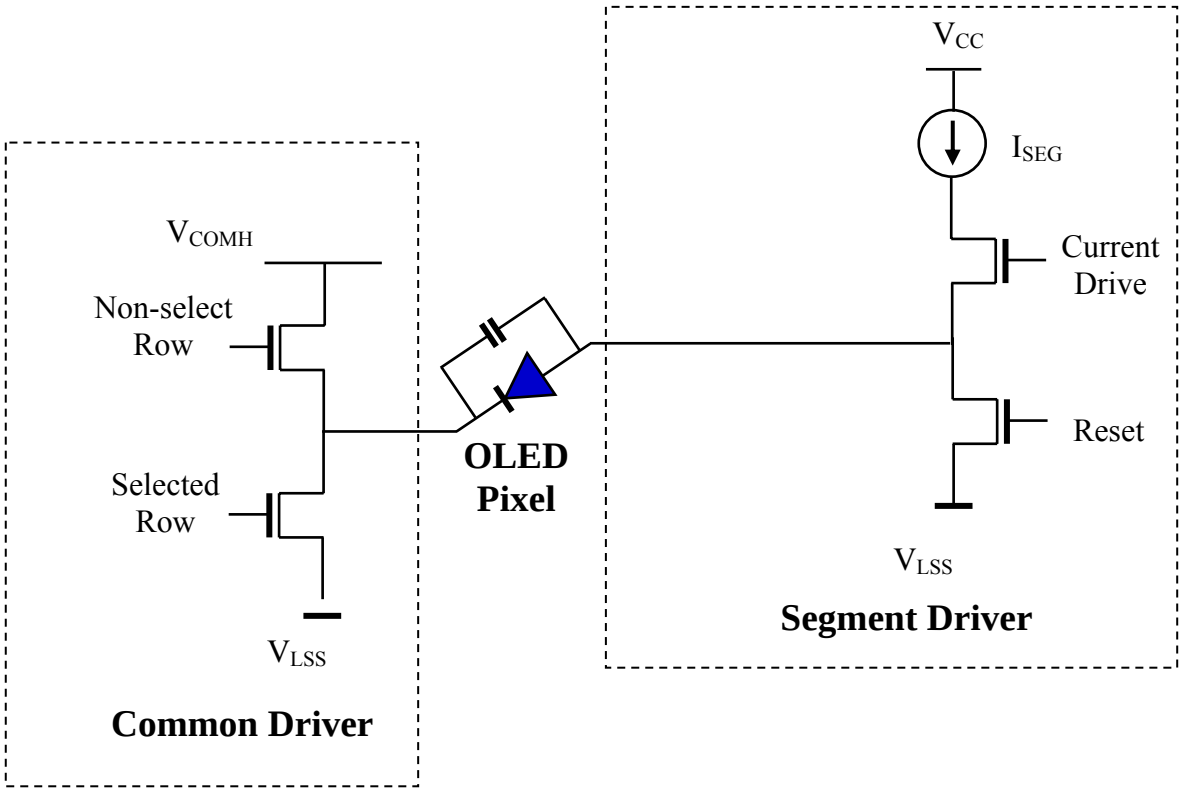
Figure 8-5: Display data write procedure in SPI mode



8.2 Segment Drivers/Common Drivers

Segment drivers have 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 8 bits, 256 steps. Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

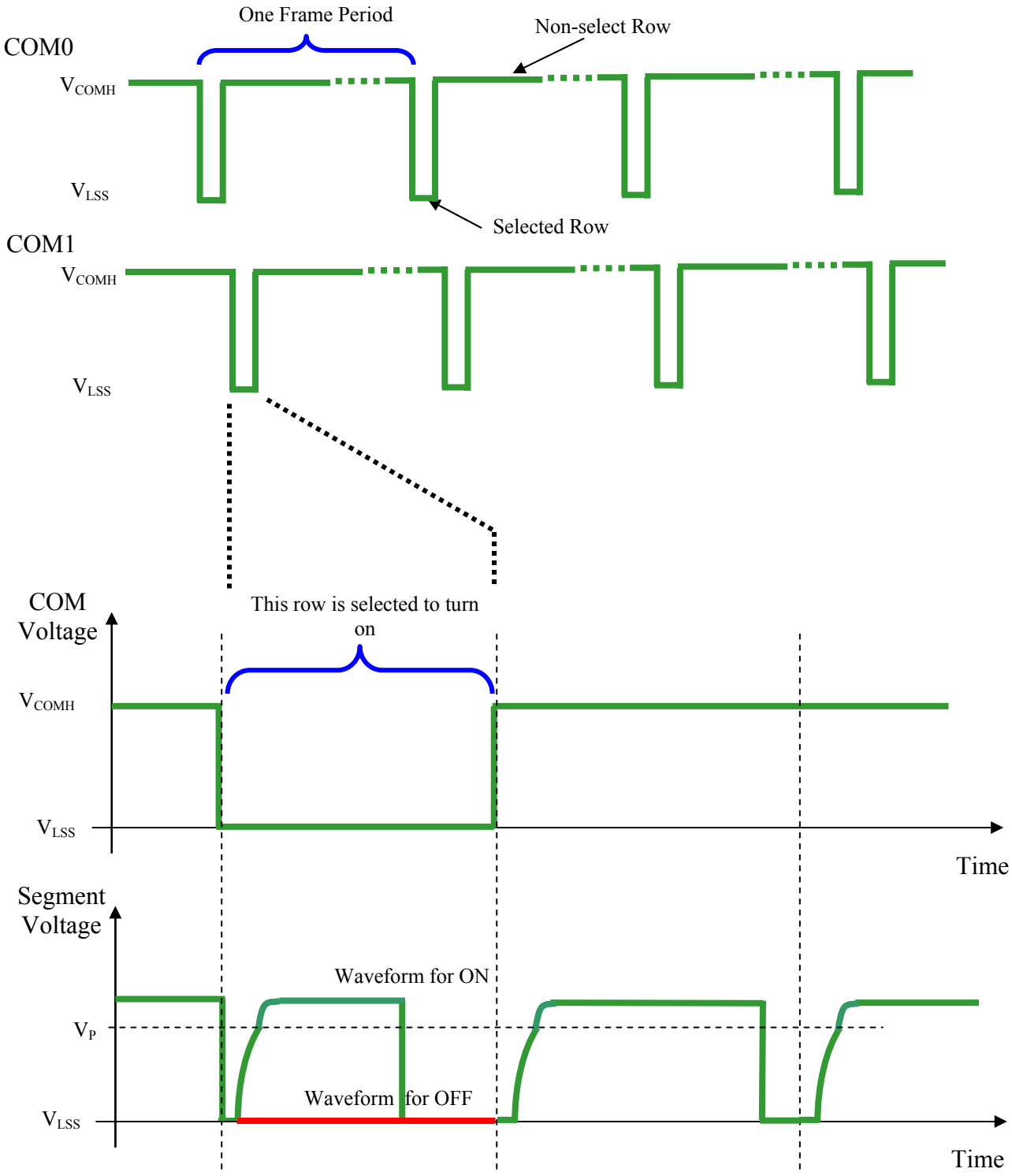
Figure 8-6: Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-7.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-7: Segment and Common Driver Signal Waveform



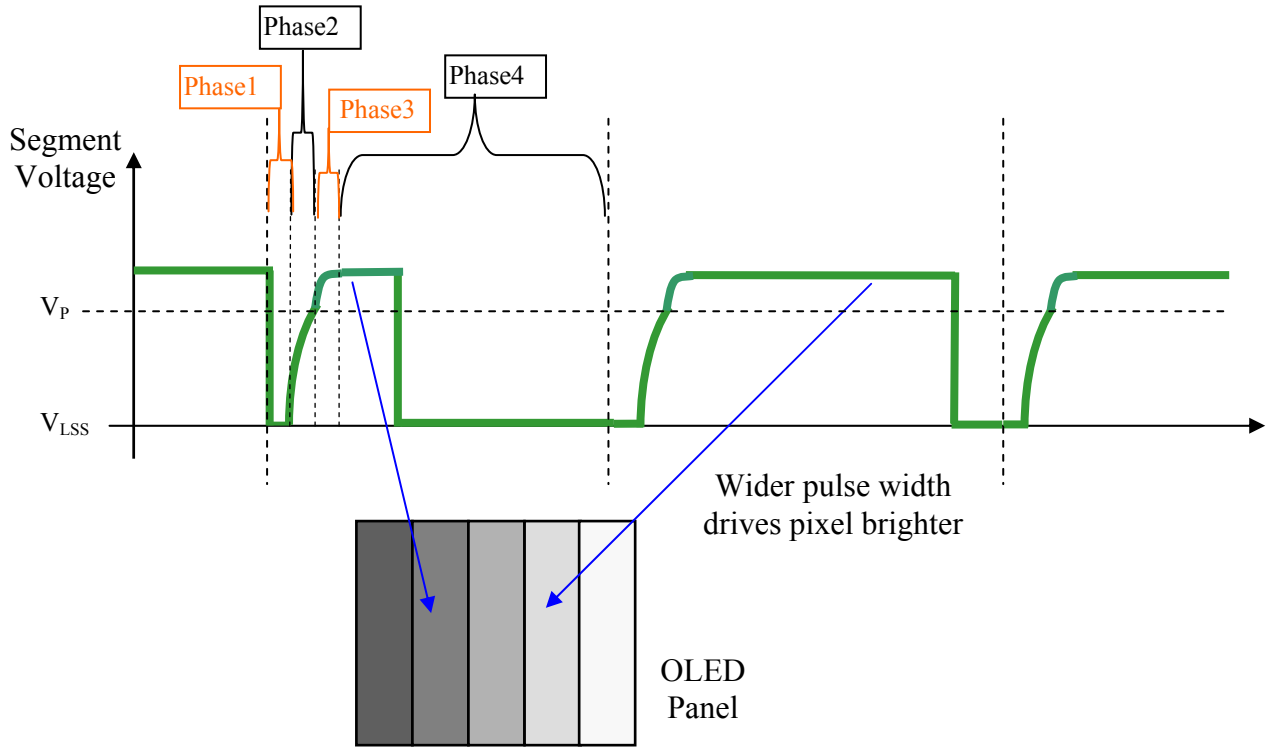
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 15 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed in length from 1 to 15 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command BBh.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

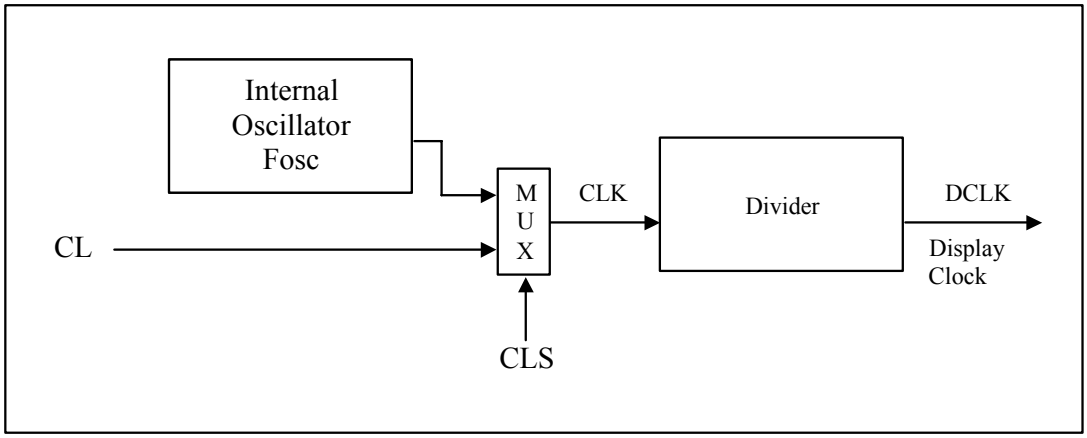
Figure 8-8: Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.
The pulse width, which is counted from Phase 2 to Phase 4, is defined by command B7h "Set Default Gray Scale Table" or B8h "Set Gray Scale Table". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-9: Oscillator Circuit and Display Time Generator



This module is an On-Chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{OSC} can be changed by command B3h, please refer to Table 9-1.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is row period. It is configured by command B2h. This value should comply with following condition.

  $$K \geq \text{Phase 1} + \text{Phase 2} + \text{Phase 3} + \text{GS15}$$
- Number of multiplex ratio is set by command A8h. The power ON reset value is 7Fh.
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in faster frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.4 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, [7:0] is treated as either the data bytes of multiple byte command or display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 128 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h

8.6 Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. I_{REF} is a reference current source for segment current drivers.

8.7 Hard icons column and row drivers

There are 64 segment drivers as the current sources to hard icons and 2 common drivers with 2 pins each to sink the current. The hard icons drivers support either DC or AC driving method.

8.8 DC-DC converter for Hard icons

It is a 2X charge-pump type voltage generator circuit. It doubles the voltage input V_{CI} to generate V_{ICON}. V_{ICON} is the voltage supply to the hard icons driver.

8.9 Gray Scale Decoder

In SSD1329 there are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2,3) and current drive (phase 4).

8.10 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 8-6 to Table 8-10 show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0 ,D1, D2, …,D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

Table 8-6 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-6: GDDRAM Address Map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

Nibble Re-map A[1]=0

Table 8-7 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-7: GDDRAM Address Map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]
|	|								
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs Column Address (HEX)

COM Outputs / Row Address (HEX)

(Display Startline=0)

Nibble Re-map A[1]=0

Table 8-8 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-8: GDDRAM Address Map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|									
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]

SEG Outputs

Column Address

(HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble Re-map A[1]=1

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. The Table 8-9 shows the example in which the display start line register is set to 78h with the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

Table 8-9: GDDRAM Address Map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM121	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs

Column Address

(HEX)

COM Outputs

Row Address (HEX)

(Display Startline=78h)

Nibble Re-map A[1]=0

Table 8-10 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

Table 8-10: GDDRAM Address Map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs Column Address (HEX)

COM Outputs (Display Startline=0)

Row Address (HEX)

Nibble Re-map A[1]=0

Note

(1) Please refer to Table 9-1 for the details of setting command “Set Re-map”A0h.

(2) The “Display Start Line” is set by the command “Set Display Start Line” A1h and please refer to Table for the setting details

(3) The “Column Start/End Address” is set by the command “Set Column Address” 15h and please refer to Table 9-1 for the setting details

(4) The “Row Start/End Address” is set by the command “Set Row Address” 75h and please refer to Table 9-1 for the setting details

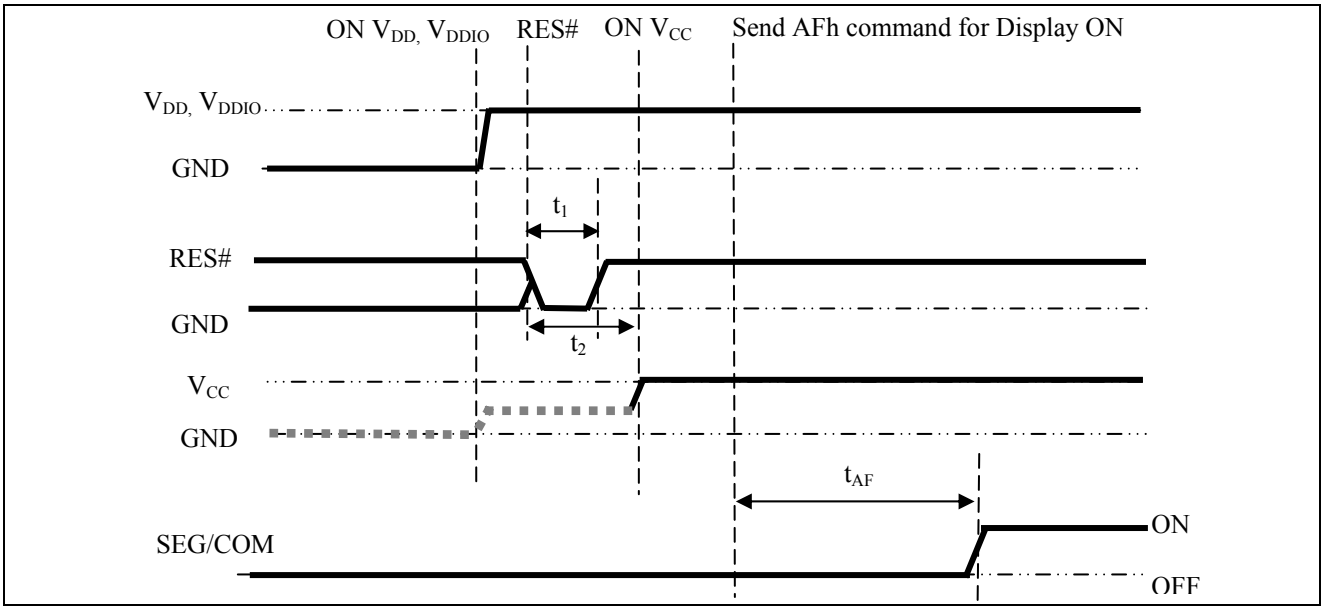
8.11 Power ON and OFF Sequence

The following figures illustrate the power ON and power OFF sequence of SSD1329 (assume V_{DD} and V_{DDIO} are at the same voltage level and hard icon is not used).

Power ON sequence:

1. Power ON $V_{DD,}$ $V_{DDIO.}$
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON $V_{CC.}$[(1)]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100us (t_{AF}).

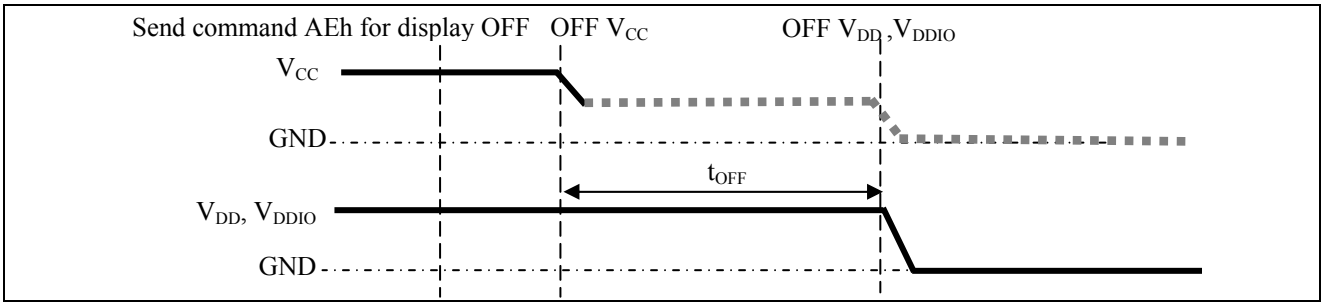
Figure 8-10: The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC.}$[(1), (2)]
3. Wait for t_{OFF}. Power OFF $V_{DD,}$ $V_{DDIO.}$ (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 8-11: The Power OFF sequence



Note:

(1) Since an ESD protection circuit is connected between $V_{DD,}$ V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} are ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-10 and Figure 8-11.

(2) V_{CC} should be kept float (disable) when it is OFF.

(3) Power Pins ($V_{DD,}$ $V_{DDIO,}$ V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) $V_{DD,}$ V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

9 COMMAND TABLE

Table 9-1: Command Table

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup Column start and end address A[5:0]: Start Address, range:00h~3Fh, (RESET = 00h) B[5:0]: End Address, range:00h~3Fh, (RESET = 3Fh) Please refers to Section 8.10 Graphic Display Data RAM (GDDRAM) for relationship between Column Address setting and GDDRAM structure.
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Setup Row start and end address A[6:0]: Start Address, range:00h~7Fh, (RESET = 00h) B[6:0]: End Address, range:00h~7Fh, (RESET = 7Fh) Please refers to 8.10 Graphic Display Data RAM (GDDRAM) for relationship between Row Address setting and GDDRAM structure.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	A[7:0]: Set Contrast Value, range:0~ 255, (RESET = 80h)
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Second Pre-charge Speed	A[7:1]: Set Second Pre-charge Speed A[7:1] = 0000000b, Second Pre-charge speed = 1 A[7:1] = 0000001b, Second Pre-charge speed = 3 : A[7:1] = 1111111b, Second Pre-charge speed = 255 The RESET value of A[7:1] depends on the value of the contrast current (81h) and is equal to: 2*81h A[7:0] +1 (maximum 7Fh) A[0] = 0, Disable doubling the Second Pre-charge speed (RESET) A[0] = 1, Enable doubling the Second Pre-charge speed Please refer to Figure 10-3 for the illustration of difference Second Pre-charge speed settings.
0 0	90 A[7:0]	1 *	0 *	0 A_5	1 A_4	0 *	0 *	0 A_1	0 A_0	Set Master Icon Control	A[1:0]: Icon control A[1:0] = 00b, Icon RESET to normal display (RESET) A[1:0] = 01b, Icon All ON (without altering icon ON / OFF register) A[1:0] = 10b, Icon All OFF (without altering icon ON/ OFF register) A[4] = 0b, Disable icon display (RESET) A[4] = 1b, Enable icon display A[5] = 0b, Disable V_{ICON} charge pump circuit (RESET) A[5] = 1b, Enable V_{ICON} charge pump circuit

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	91 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Icon Current Range	A[7:0]: Set Icon current range A[7:0] = 00h, max icon current = 0.0uA A[7:0] = 01h, max icon current = 0.5uA A[7:0] = 02h, max icon current = 1.0uA A[7:0] = 03h, max icon current = 1.5uA A[7:0] = 04h, max icon current = 2.0uA … … A[7:0] = FCh, max icon current = 126.0uA A[7:0] = FDh, max icon current = 126.5uA A[7:0] = FEh, max icon current = 127.0uA A[7:0] = FFh, max icon current = 127.5uA (RESET) **Note** (1) The larger the icon current range is, the better the uniformity is.
0 0 0 … … 0 0	92 A0[6:0] A1[6:0] … … A62[6:0] A63[6:0]	1 * * … … * *	0 $A0_6$ $A1_6$ … … $A62_6$ $A63_6$	0 $A0_5$ $A1_5$ … … $A62_5$ $A63_5$	1 $A0_4$ $A1_4$ … … $A62_4$ $A63_4$	0 $A0_3$ $A1_3$ … … $A62_3$ $A63_3$	0 $A0_2$ $A1_2$ … … $A62_2$ $A63_2$	1 $A0_1$ $A1_1$ … … $A62_1$ $A63_1$	0 $A0_0$ $A1_0$ … … $A62_0$ $A63_0$	Set Individual Icon Current	Set each Icon current by the formula: (AN[6:0] / 127) x max icon current, where the max icon current is defined by the command "Set icon current range" 91h and N=0~63. e.g. Icon Current of ICS0 = (A0[6:0]/127) x max icon current. A0[6:0]: icon current for ICS0, range: 00h~7Fh A1[6:0]: icon current for ICS1, range: 00h~7Fh … … A62[6:0]: icon current for ICS62, range: 00h~7Fh A63[6:0]: icon current for ICS63, range: 00h~7Fh **Note** (1) All 64 levels (1 level for each ICS signals) of icon current must be entered, in order to operate this command properly. (2) The icon current of the unused icon pins must be set to zero by this command.
0 0	93 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Individual Icon ON / OFF Register	Individual icon selection: A[5:0]: select one of the 64 icons from ICS0 ~ ICS63 A[7:6] = 00b, turn OFF selected icon A[7:6] = 01b, turn ON selected icon A[7:6] = 11b, blink selected icon e.g A[7:0] = 01000000b, turn ON icon ICS0 A[7:0] = 00111111b, turn OFF icon ICS63
0 0	94 A[7:6]	1 A_7	0 A_6	0 *	1 *	0 *	1 *	0 *	0 *	Set Icon ON / OFF Registers	A[7:6]: Master control of Icon register A[7:6] = 00b, turn OFF all icon A[7:6] = 01b, turn ON all icon A[7:6] = 11b, blink all icons

Fundamental Command Table

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0</td><td>95
A[7:0]</td><td>1
*</td><td>0
*</td><td>0
0</td><td>1
1</td><td>0
*</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Icon Blinking Cycle</td><td>A[2:0]: Set Icon blinking cycle:
<table><tr><td>A[2:0]</td><td>blinking cycle</td><td>A[2:0]</td><td>blinking cycle</td></tr><tr><td>000b</td><td>0.25sec</td><td>100b</td><td>1.25sec</td></tr><tr><td>001b</td><td>0.50sec</td><td>101b</td><td>1.50sec</td></tr><tr><td>010b</td><td>0.75sec</td><td>110b</td><td>1.75sec</td></tr><tr><td>011b</td><td>1.00sec(RESET)</td><td>111b</td><td>2.00sec</td></tr></table>Note
(1) Blinking cycles is measured at reset icon frame frequency and duty ratio of 50% (refer to Figure 10-4 for the meaning of 50% duty ratio)
(2) There is 10% tolerance in the above blinking cycle values.
(3) A[5:4] must be set to 01b.</td></tr>
<tr><td>0
0</td><td>96
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>0
A_5</td><td>1
A_4</td><td>0
*</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Icon Driving Scheme and Icon Frame Frequency</td><td>A[2:0]: Set icon DC drive / AC drive duty ratio
000b DC drive (RESET)
001b 63 / 64 duty ratio
010b 62 / 64 duty ratio
011b 61 / 64 duty ratio
100b 60 / 64 duty ratio
101b 59 / 64 duty ratio
110b 58 / 64 duty ratio
111b 57 / 64 duty ratio

A[7:4]: Set icon frame frequency

The icon frame frequency (F_{IFRM}) is calculated by this formula:
$$F_{IFRM} = \frac{64000}{64 \times (A[7:4]+1)}$$
where A[7:4] is ranged from 8~15 as follow.
<table><tr><td colspan="4">A[7:4] setting</td></tr><tr><td>0101b</td><td>5d</td><td>1011b</td><td>11d</td></tr><tr><td>0110b</td><td>6d</td><td>1100b</td><td>12d</td></tr><tr><td>0111b</td><td>7d</td><td>1101b</td><td>13d</td></tr><tr><td>1000b</td><td>8d</td><td>1110b</td><td>14d</td></tr><tr><td>1001b</td><td>9d (RESET)</td><td>1111b</td><td>15d</td></tr><tr><td>1010b</td><td>10d</td><td></td><td></td></tr></table>Example: when in default case,
$$F_{IFRM} = \frac{64000}{64 \times (9+1)} = 100Hz$$
Note
(1) Icon frame frequency must NOT be set to 0000b.
(2) There is 10% tolerance in the above frequency value</td></tr>
</table>

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map	Re-map setting in Graphic Display Data RAM (GDDRAM) A[7:0]: Remap (RESET = 00h) A[0] = 0b, Disable Column Address Re-map (RESET) A[0] = 1b, Enable Column Address Re-map A[1] = 0b, Disable Nibble Re-map (RESET) A[1] = 1b, Enable Nibble Re-map A[2] = 0b, Enable Horizontal Address Increment (RESET) A[2] = 1b, Enable Vertical Address Increment A[4] = 0b, Disable COM Re-map (RESET) A[4] = 1b, Enable COM Re-map A[6] = 0b, Disable COM Split Odd Even (RESET) A[6] = 1b, Enable COM Split Odd Even
0 0	A1 A[7:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	A[6:0]: Vertical shift by setting the starting address of display RAM from 0 ~ 127 (RESET = 00h)
0 0	A2 A[7:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	A[6:0]: Set vertical offset by COM from 0 ~ 127 (RESET = 00h) e.g. Set A[6:0] to 010000b to move COM16 towards COM0 direction for 16 row
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4: Normal display (RESET) A5: All ON (All pixels have gray scale of 15, GS15) A6: All OFF (All pixels have gray scale of 0, GS0) A7: Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 0	A8 A[6:0]	0 *	0 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX: A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 126 represents 127MUX A[6:0] = 127 represents 128MUX (RESET) It should be noted that A[6:0]=0~14 is not allowed.
0 0	AE AF	1 1	0 0	1 1	0 0	1 1	1 1	1 1	0 1	Set Sleep mode ON / OFF	A[0] = 0b, Sleep mode ON (The display is OFF) A[0] = 1b, Sleep mode OFF (The display is ON)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[7:0]: RESET and first pre-charge phase length (RESET=53h) A[3:0]: Phase 1 period of 1~15 DCLK's (RESET=3h) e.g. A[3:0] = 1111b, 15 DCLK Clock A[7:4]: Phase 2 period of 1~15 DCLK's (RESET=5h) e.g. A[7:4] = 1111b, 15 DCLK Clocks **Note** (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[6:0]	1 *	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Frame Frequency	Set the frame frequency of the matrix display A[6:0]:Total number of DCLK's per row. Ranging from 14h to 4Eh DCLK's (RESET = 23h) Then the frame Frequency = DCLK freq /A[6:0]. **Note** (1) It is recommend to set B2 A[6:0] to B1 A[3:0] + pulse width of GS15
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Front Clock Divider /Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) Divide ratio=A[3:0]+1 (RESET is 0000b, i.e. divide ratio = 1) A[7:4]: Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. Range:0h~Fh (RESET= 0h represents 500KHz, typical step value: 4% of previous value)
0	B7	1	0	1	1	0	1	1	1	Set Default Gray Scale Table	The default gray scale table is set in unit of DCLKs as follow: GS1 level Pulse width = 2 DCLKs GS2 level Pulse width = 4 DCLKs GS3 level Pulse width = 6 DCLKs … … … GS13 level Pulse width = 26 DCLKs GS14 level Pulse width = 28 DCLKs GS15 level Pulse width = 30 DCLKs **Note** (1) The pulse width is counted from Phase 2 to Phase 4. (2) The pulse width DCLKs of each GS is bounded by above values in spite of the settings in Phase 2 period and Phase 3 period (refer to command B1h, BBh)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	Set gray scale (GS1~GS15) pulse width in unit of DCLKs. A1[5:0], value for GS1 level Pulse width A2[5:0], value for GS2 level Pulse width … A14[5:0], value for GS14 level Pulse width A15[5:0], value for GS15 level Pulse width **Note** (1) The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15 (2) The pulse width is counted from Phase 2 to Phase 4. (3) The pulse width DCLKs of each GS is bounded by above settings in spite of the settings in Phase 2 period and Phase 3 period (refer to command B1h, BBh)
0	A1[5:0]	*	*	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
0	A2[5:0]	*	*	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
…	…	…	…	…	…	…	…	…	…		
…	…	…	…	…	…	…	…	…	…		
…	…	…	…	…	…	…	…	…	…		
0	A14[5:0]	*	*	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
0	A15[5:0]	*	*	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
0	BB	1	0	1	1	1	0	1	1	Set Second Pre-charge Period	A[3:0]: Set Second pre-charge period 0000b 0 DCLK 0001b 1 DCLKs 0010b 2 DCLKs : 0111b 7 DCLKs (RESET) : 1111b 15 DCLKs
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	BC	1	0	1	1	1	1	0	0	Set First Pre-charge voltage, V_P	A[5:0]: Set First Pre-charge voltage 000000b 0.30 x V_{CC} 000001b 0.31 x V_{CC} … … 001111b 0.45 x V_{CC} (RESET) … … 011111b 0.63 x V_{CC} 1xxxxxb 1.00 x V_{CC} or connect to V_{COMH} if $V_{CC} > V_{COMH}$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	A[4:0]: Output level high voltage for COM signal 00000b 0.51 x V_{CC} 01000b 0.58 x V_{CC} 10000b 0.66 x V_{CC} 11000b 0.75 x V_{CC} 11111b 0.84 x V_{CC} (RESET)
0	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
0	A[2]	0	0	0	1	0	A_2	1	0		

Note
(1) "*" stands for "Don't care".

Table 9-2: Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	23	0	0	1	0	0	0	1	1	Graphic Acceleration Command Options	A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET) A[1] = 0b: Disable x-wrap A[1] = 1b: Enable wrap around in x-direction during copying and scrolling (RESET) A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0	A[4:0]	*	*	*	A_4	*	*	A_1	A_0		
0	24	0	0	1	0	0	1	0	0	Draw Rectangle	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[7:0]: Set Gray scale pattern E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 10-16 for the gray scale pattern setting examples. **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 127$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	25	0	0	1	0	0	1	0	1	Copy	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[5:0]: Column Address of New Start F[6:0]: Row Address of New Start **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 127$ (3) $0 \le E \le 63$ (4) $0 \le F \le 127$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[6:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	26	0	0	1	0	0	1	1	0	Horizontal and Vertical Scroll	A[5:0]: 1~63 horizontal offset in number of 2~126 column 0 no horizontal scroll B[6:0]: 0~127 start row address for horizontal scroll C[1:0]: scrolling time interval 00b 6 frames 01b 10 frames 10b 100 frames 11b 200 frames D[7:0]: number of rows to be H-scrolled B+D <= 128 E[6:0]: 1~63 simultaneous continuous vertical scroll offset in number of row 0 no vertical scroll **Note:** (1) Scrolling operates during display on. (2) The parameters should not be changed after scrolling is activated
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[6:0]	*	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	2E	0	0	1	0	1	1	1	0	Stop Moving	This command deactivates the scrolling action. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal & Vertical Scroll command 26h.

Table 9-3: Read Command Table

(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7]=0:reserved D[7]=1:reserved D[6]=0:indicates the display is ON D[6]=1:indicated the display is OFF D[5]=0:reserved D[5]=1:reserved D[4]=0:reserved D[4]=1:reserved

Note

(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

9.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, input LOW to R/W# (WR#) pin and HIGH to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

Table 9-4: Address Increment Table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Fundamental command description

10.1.1 Set Column Address (15h)

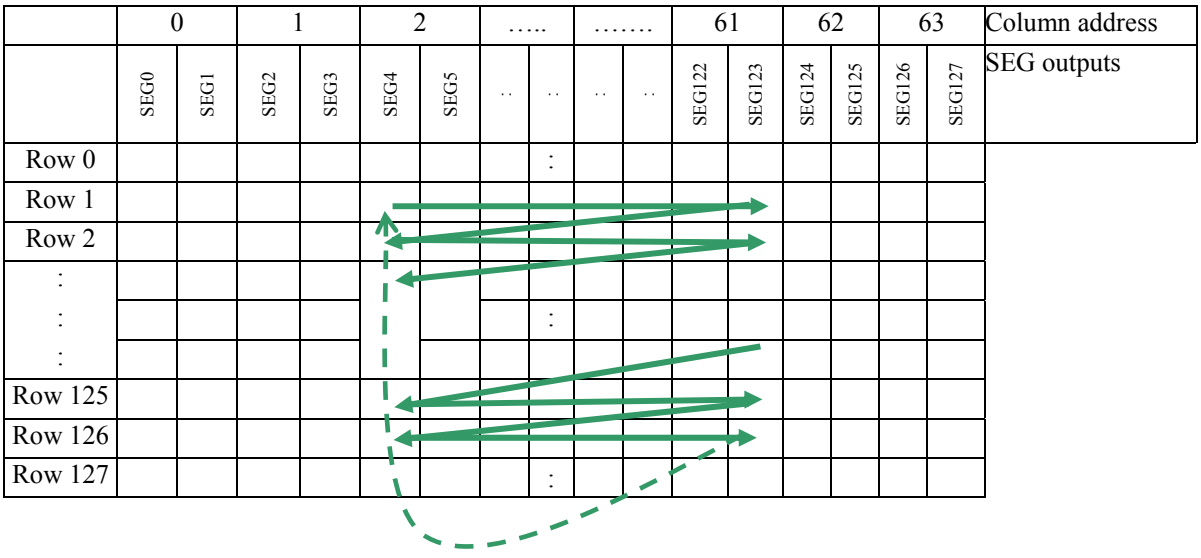
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 61, row start address is set to 1 and row end address is set to 126; horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 61 and from row 1 to row 126 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-1*). Whenever the column address pointer finishes accessing the end column 61, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in Figure 10-1*). While the end row 126 and end column 61 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2 (*dotted line in Figure 10-1*). .

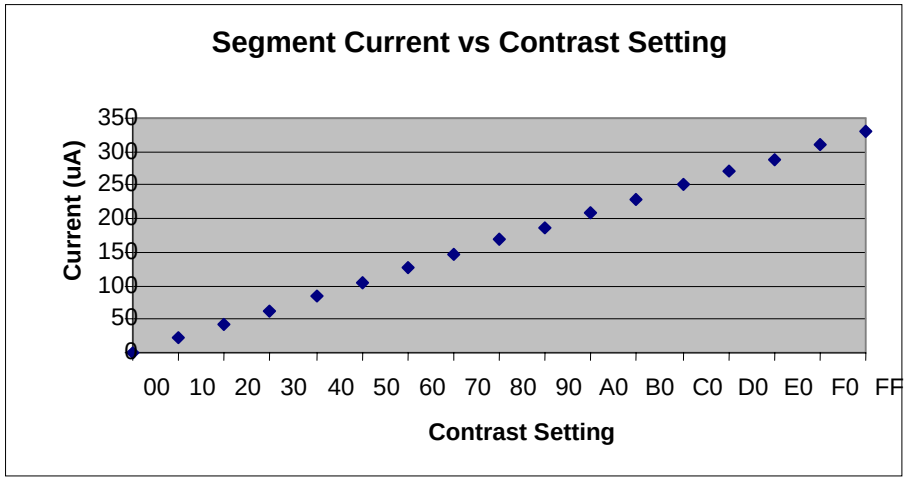
Figure 10-1: Example of Column and Row Address Pointer Movement



10.1.3 Set Contrast Current (81h)

This double byte command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current increases with the increase of contrast step

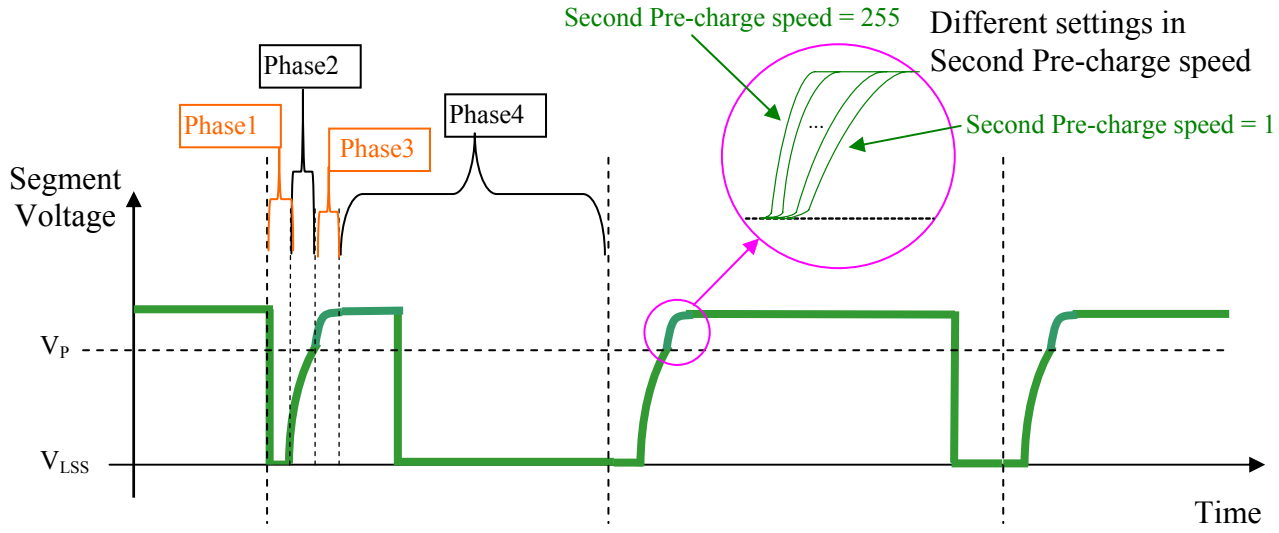
Figure 10-2: Example of Segment current versus Contrast setting



10.1.4 Set Second Pre-charge Speed (82h)

This command is used to set the speed of second pre-charge in phase 3. This speed can be doubled to achieve faster pre-charging through setting 82h A[0]. Please refer to Table 9-1: Command Table for the details of setting. Figure 10-3 shows the effect of setting second pre-charge under different speeds through using command 82h.

Figure 10-3: Effect of setting the second pre-charge under different speeds



10.1.5 Set Master Icon Control (90h)

This double command is used to set the ON / OFF conditions of internal charge pump, icon circuits and overall icon status.

10.1.6 Set Icon Current Range (91h)

This double byte command is used to set one fix current range for all icons between the range of 0uA and 127.5uA. The uniformity improves as the icon current range increases. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.7 Set Individual Icon Current (92h)

This double byte command is used to fine tune the current for each of the 64 icons. Command 92h followed by 64 single byte data. These 64 byte data have to be entered in order to make this command function. Below is the formula for calculating the icon current. Please also refer to Table 9-1 for detail information and breakdown levels of each step.

Icon Current = Single byte value / 127 x Maximum icon current set with command 91h.

10.1.8 Set Individual Icon ON / OFF Registers (93h)

This double byte command is used to select one of the 64 icons and choose the ON, OFF or blinking condition of the selected icon.

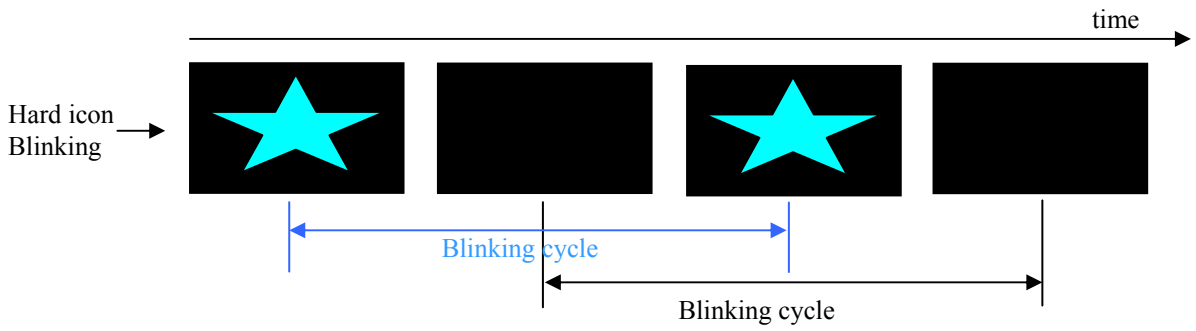
10.1.9 Set Icon ON / OFF Registers (94h)

This double byte command is used to set the ON / OFF status of all 64 icons.

10.1.10 Set Icon Blinking Cycle (95h)

This double byte command is used to set icon blinking cycle selected with above command 93h. Please refer to Table 9-1 for detail information and breakdown levels of each step.

Figure 10-4 : Hard icon Blinking cycle (50% duty ratio)



10.1.11 Set Icon Driving Scheme and Icon Frame Frequency (96h)

This double byte command is used to set the icon frame frequency and icon AC drive duty ratio. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.12 Set Re-Map(A0h)

This double command has multiple configurations and each bit setting is described as follows:

- Column Address Remapping (A[0])
  This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).

- Nibble Remapping (A[1])

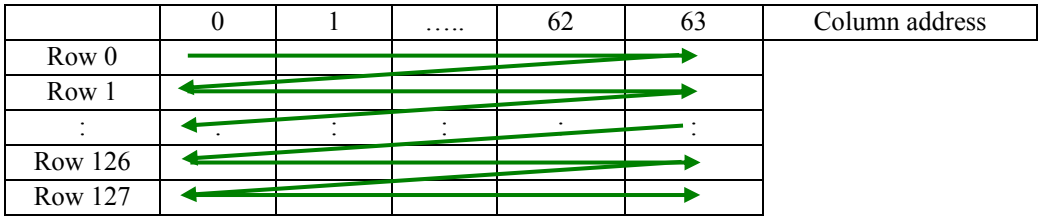
  When A[1] is set to 1, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)

  If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0~127 to SEG127~SEG0 as show in Table 8-8.

- Address increment mode (A[2])

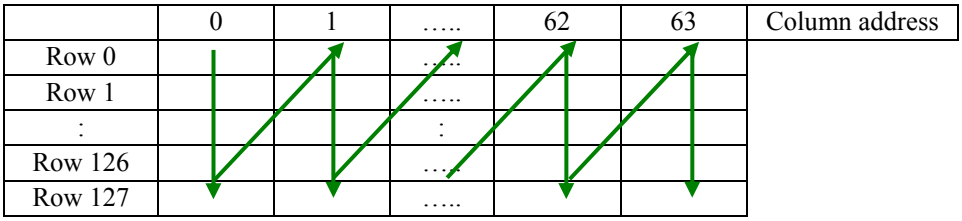
  When A[2] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-5.

Figure 10-5: Address Pointer Movement of Horizontal Address Increment Mode



When A[2] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-6.

Figure 10-6: Address Pointer Movement of Vertical Address Increment Mode

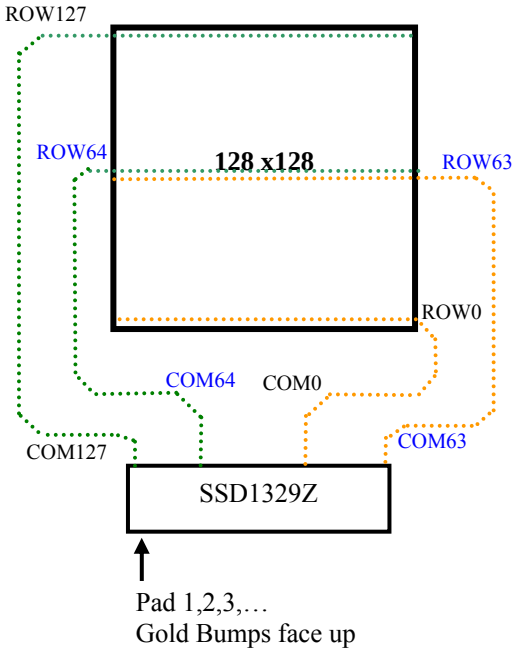


- COM Remapping (A[4])
  This bit defines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down (when A[4] is set to 0) or from bottom to up (when A[4] is set to 1). Table 8-9 shows one example of the using the COM Remapping to perform vertical scrolling.

- Splitting of Odd / Even COM Signals (A[6])
  This bit is made to match the COM layout connection on the panel.

  When A[6] is set to 0, no splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

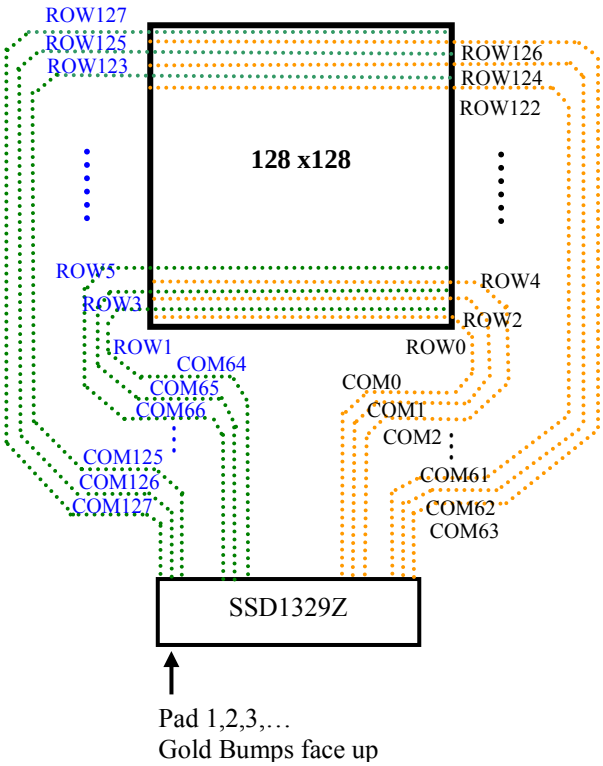
Figure 10-7: Output pin assignment when command A0h bit A[6]=0.



Output Pin Connection	
SSD1329Z	**Panel**
COM0	ROW0
COM1	ROW1
COM2	ROW2
COM3	ROW3
:	:
COM63	ROW63
COM64	ROW64
:	:
COM125	ROW125
COM126	ROW126
COM127	ROW127

When A[6] is set to 1, splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

Figure 10-8: Output pin assignment when command A0h bit A[6]=1.



Output Pin Connection	
SSD1329Z	**Panel**
COM0	ROW0 (Even)
COM1	ROW2
COM2	ROW4
:	:
COM61	ROW122
COM62	ROW124
COM63	ROW126
COM64	ROW1 (Odd)
COM65	ROW3
COM66	ROW5
:	:
COM125	ROW123
COM126	ROW125
COM127	ROW127

10.1.13 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-9 shows an example using this command of this command when MUX ratio= 128 and MUX ratio= 90 and Display Start Line = 40. In there, “ROW” means the graphic display data RAM row.

Figure 10-9: Example of Set Display Start Line with no Remapping

	MUX ratio (A8h) = 128	MUX ratio (A8h) = 128	MUX ratio (A8h) = 90	MUX ratio (A8h) = 90
COM Pin	Display Start Line (A1h) = 0	Display Start Line (A1h) = 40	Display Start Line (A1h) = 0	Display Start Line (A1h) = 40
COM0	ROW0	ROW40	ROW0	ROW40
COM1	ROW1	ROW41	ROW1	ROW41
COM2	ROW2	ROW42	ROW2	ROW42
COM3	ROW3	ROW43	ROW3	ROW43
:	:	:	:	:
:	:	:	:	:
COM48	ROW48	ROW88	ROW48	ROW88
COM49	ROW49	ROW89	ROW49	ROW89
COM50	ROW50	ROW90	ROW50	ROW90
COM51	ROW51	ROW91	ROW51	ROW91
:	:	:	:	:
:	:	:	:	:
COM86	ROW86	ROW126	ROW86	ROW126
COM87	ROW87	ROW127	ROW87	ROW127
COM88	ROW88	ROW0	ROW88	ROW0
COM89	ROW89	ROW1	ROW89	ROW1
COM90	ROW90	ROW2	-	-
COM91	ROW91	ROW3	-	-
:	:	:	:	:
:	:	:	:	:
COM124	ROW124	ROW36	-	-
COM125	ROW125	ROW37	-	-
COM126	ROW126	ROW38	-	-
COM127	ROW127	ROW39	-	-
Display Example				

10.1.14 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0~COM127. Figure 10-10 shows an example using this command when MUX ratio= 128 and MUX ratio= 90 and Display Offset = 40. In there, "Row" means the graphic display data RAM row.

Figure 10-10: Example of Set Display Offset with no Remapping

	MUX ratio (A8h) = 128	MUX ratio (A8h) = 128	MUX ratio (A8h) = 90	MUX ratio (A8h) = 90
COM Pin	Display Offset (A2h)=0	Display Offset (A2h)=40	Display Offset (A2h)=0	Display Offset (A2h)=40
COM0	ROW0	ROW40	ROW0	ROW40
COM1	ROW1	ROW41	ROW1	ROW41
COM2	ROW2	ROW42	ROW2	ROW42
COM3	ROW3	ROW43	ROW3	ROW43
:	:	:	:	:
:	:	:	:	:
COM48	ROW48	ROW88	ROW48	ROW88
COM49	ROW49	ROW89	ROW49	ROW89
COM50	ROW50	ROW90	ROW50	-
COM51	ROW51	ROW91	ROW51	-
:	:	:	:	:
:	:	:	:	:
COM86	ROW86	ROW126	ROW86	-
COM87	ROW87	ROW127	ROW87	-
COM88	ROW88	ROW0	ROW88	ROW0
COM89	ROW89	ROW1	ROW89	ROW1
COM90	ROW90	ROW2	-	R0W2
COM91	ROW91	ROW3	-	ROW3
:	:	:	:	:
:	:	:	:	:
COM124	ROW124	ROW36	-	ROW36
COM125	ROW125	ROW37	-	ROW37
COM126	ROW126	ROW38	-	ROW38
COM127	ROW127	ROW39	-	ROW39
Display Example				

10.1.15 Set Display Mode (A4h ~ A7h)

These are single byte commands and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display.

- Normal Display (A4h)
  Reset the "Entire Display ON, Entire Display OFF or Inverse Display" effects and turn the data to ON at the corresponding gray level. Figure 10-11 shows an example of Normal Display.

Figure 10-11: Example of Normal Display

Memory Display

- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM. Figure 10-12

Figure 10-12: Example of Entire Display ON

Memory Display

- Set Entire Display OFF (A6h)
  Force the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM. Figure 10-13

Figure 10-13: Example of Entire Display OFF

Memory Display

- Inverse Display (A7h)
  The gray scale level of display data are swapped such that "GS0" <-> "GS15", "GS1" <-> "GS14", etc. Figure 10-14 shows an example of inverse display.

Figure 10-14: Example of Inverse Display

Memory Display

10.1.16 Set MUX Ratio (A8h)

This double byte command sets multiplex ratio (MUX ratio) from 16MUX to 128MUX. In RESET, multiplex ratio is 128MUX. Please refer to Figure 10-9 and Figure 10-10 for the example of setting different MUX ratio.

10.1.17 Set Sleep Mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the matrix display on the OLED panel display either ON or OFF. When the sleep mode is set to ON (AEh), the display is OFF, the segment and common output are in high impedance state and circuits will be turned OFF. When the sleep mode is set to OFF (AFh), the display is ON.

10.1.18 Set Phase Length (B1h)

In the second byte of this double command, lower nibble and higher nibble is defined separately. The lower nibble adjusts the phase length of Reset (phase 1). The higher nibble is used to select the phase length of first pre-charge phase (phase 2). The phase length is ranged from 1 to 16 DCLK's.
RESET for A[3:0] is set to 3h which means 4 DCLK's selected for Reset phase. RESET for A[7:4] is set to 5h which means 6 DCLK's is selected for first pre-charge phase. Please refer to Table 9-1 for detail breakdown levels of each step.

10.1.19 Set Frame Frequency (B2h)

This double byte command is used to set the number of DCLK's per row between the range of 14h and 7Fh. Then the Frame frequency of the matrix display is equal to DCLK frequency / A[6:0].

10.1.20 Set Front Clock Divider / Oscillator Frequency (B3h)

This double command is used to set the frequency of the internal display clocks, DCLK's. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. The lower nibble of the second byte is used to select the oscillator frequency. Please refer to Table 9-1 for detail breakdown levels of each step.

10.1.21 Set Default Gray Scale Table (B7h)

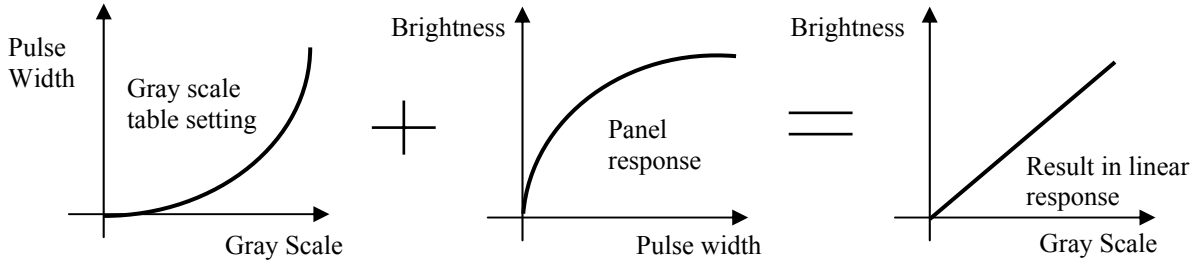
This single byte command is used to set the gray scale table to initial default setting.

10.1.22 Look Up Table for Gray Scale Pulse width (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale level GS0 that has no pre-charge and current drive, the pulse width of each gray scale level is programmed with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 10-15: Example of gamma correction by gray scale table setting



10.1.23 Set Second Pre-charge period (BBh)

This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command BBh and it is ranged from 0 to 15 DCLK's. Please refer to Table 9-1 for the details of setting.

10.1.24 Set First Pre-charge voltage, V_P (BCh)

This double byte command is used to set phase 2 first pre-charge voltage level. It can be programmed to set the first pre-charge voltage reference to V_{CC} or V_{COMH}. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.25 Set V_{COMH} (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.1.26 No Operation (E3h)

This is a no operation command.

10.1.27 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

10.2 Graphic Acceleration Command Set Description

10.2.1 Graphic Acceleration Command Options (23h)

This command has two functions.

- Enable / Disable fill (A[0])
  0 = Disable filling of rectangle in draw rectangle command.
  1 = Enable filling of rectangle in draw rectangle command. (RESET)

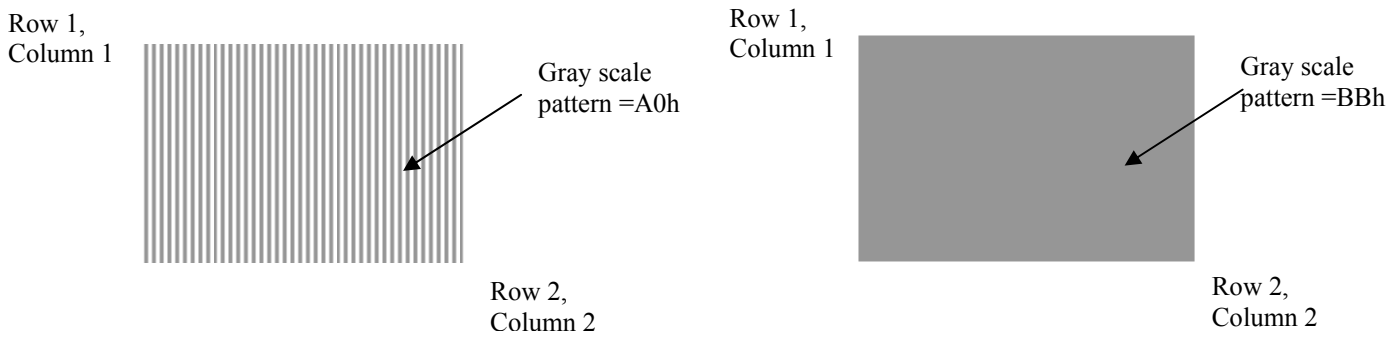
- Enable / Disable x-warp (A[1])
  0 = Disable wrap around in x-direction during copying and scrolling
  1 = Enable wrap around in x-direction during copying and scrolling (RESET)

- Enable / Disable reverse copy (A[4])
  0 = Disable reverse copy (RESET)
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS15", "GS1" <-> "GS14", ….

10.2.2 Draw Rectangle (24h)

Specify a starting point (Row 1, Column 1) and an ending point (Row 2, Column 2) as well as giving the desire gray scale pattern, a rectangle will then be drawn.

Figure 10-16: Example of draw rectangle command



The following example illustrates the rectangle drawing command sequence.

1. Enter the "draw rectangle mode" by execute the command 24h
2. Set the starting column coordinates, Column 1. e.g., 01h.
3. Set the starting row coordinates, Row 1. e.g., 01h.
4. Set the finishing column coordinates, Column 9. e.g., 09h
5. Set the finishing row coordinates, Row 5. e.g., 05h
6. Set the gray scale pattern:
   This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 10-16 for the gray scale pattern setting examples.

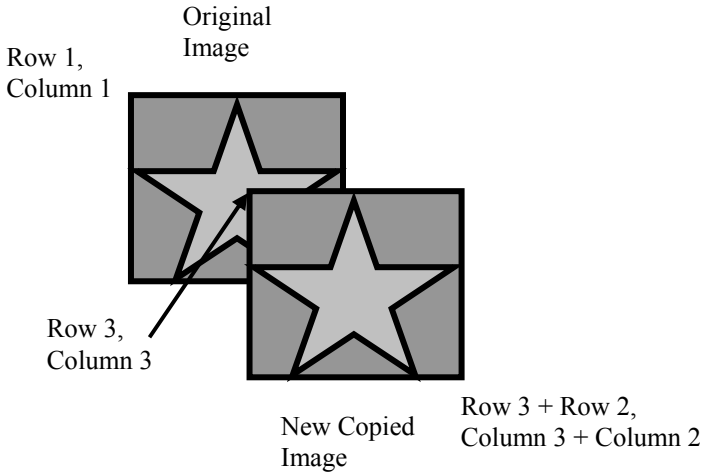
10.2.3 Copy (25h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 25h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

Figure 10-17: Example of copy command

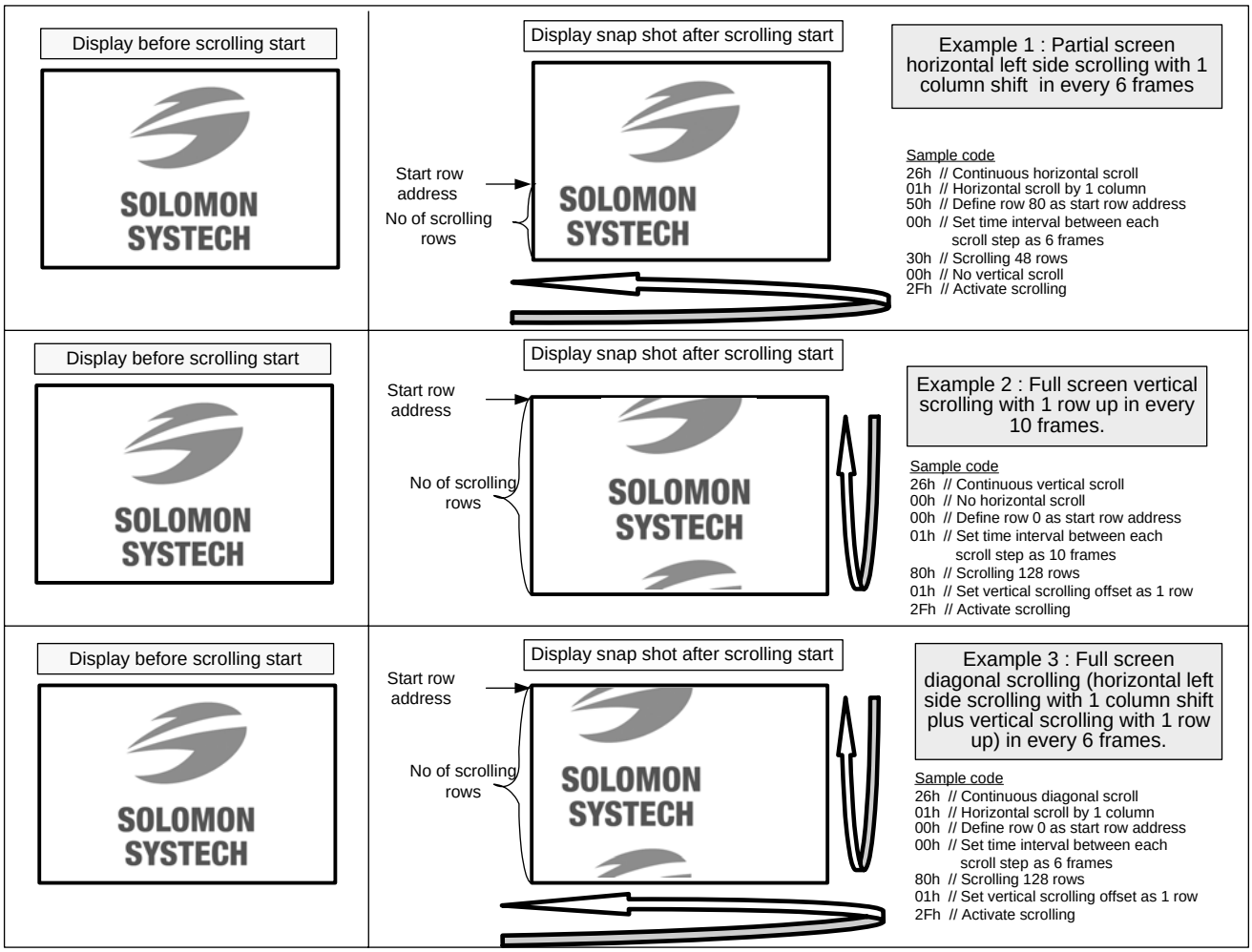


10.2.4 Horizontal and Vertical Scroll (26h)

This command consists of 5 consecutive bytes to set up the scrolling parameters. It determined the horizontal scrolling start and end row, scrolling offset and scrolling speed. Some scrolling examples are shown in Figure 10-18 .

Before issuing this command, the scrolling must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

Figure 10-18: Scrolling examples



10.2.5 Stop Moving (2Eh)

Stop motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.6 Start Moving (2Fh)

Start motion of scrolling. This command should only be issued after scrolling setup parameters are defined.

The following actions are prohibited after the horizontal scroll is activated

1. RAM access (Data write or read)
2. Changing scrolling setup parameters

11 MAXIMUM RATINGS

Table 11-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{DDIO}		-0.3 to +4.0	V
V_{CC}		0 to +19.0	V
V_{SEG}	SEG output voltage	0 to + V_{CC}	V
V_{COM}	COM output voltage	0 to + 0.9*V_{CC}	V
V_{IN}	Input voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{STG}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (unless specified):

Voltage referenced to V_{SS};

V_{DD} = 2.7, V_{DDIO} = 1.8V, V_{CC} = 11.0V, V_{CI} = 3.5V, I_{REF} = 10uA, at T_A = 25°C.

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	9.0	11.0	18.0	V
V_{DD}	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.7	1.8	V_{DD}	V
V_{CI}	Charge Pump Supply Voltage	-	3.2	3.5	4.2	V
V_{ICON}	Icon Supply Voltage	-	6.4	7.0	8.4	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level		0	-	0.1 x V_{DDIO}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2 x V_{DDIO}	V
$I_{DD, SLEEP}$	Sleep mode V_{DD} Current	Display OFF, No panel attached	-5	0	5	uA
$I_{DDIO, SLEEP}$	Sleep mode V_{DDIO} Current		-5	0	5	uA
$I_{CC, SLEEP}$	Sleep mode V_{CC} Current		-5	0	5	uA
I_{DD}	V_{DD} Supply Current	Display ON, All 1's pattern, Contrast = 80h, No panel attached	25	40	55	uA
I_{CC}	V_{CC} Supply Current		400	440	480	uA
I_{DD}	V_{DD} Supply Current	Display ON, All 0's pattern, Contrast = 80h, No panel attached	25	40	55	uA
I_{CC}	V_{CC} Supply Current		80	100	120	uA
I_{SEG}	Segment Output Current: Display ON, All 1's pattern (Segment pin under test is connected with a 20K Ω resistive load to V_{SS})	Contrast = FFh	280	310	340	uA
		Contrast = 7Fh	135	150	165	uA
		Contrast = 3Fh	68	75	82	uA
Dev	Segment Output Current Uniformity: Dev = $(I_{SEG} - I_{MID}) / I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ I_{SEG} [0:127] = Segment current at contrast settings	Contrast = FFh	-3.0	-	+3.0	%
		Contrast = 7Fh				
		Contrast = 3Fh				
Adj. Dev	Adjacent pin output current uniformity: Adj Dev = (I[n] - I[n+1]) / (I[n]+I[n+1])	Contrast = FFh	-2.0	-	+2.0	%
		Contrast = 7Fh				
		Contrast = 3Fh				
I_{SEG}	IC-to-IC Segment Output Current Uniformity: Display ON, All 1's pattern (Segment pin under test is connected with a 20K Ω resistive load to V_{SS})	Contrast = FFh	-10.0	-	+10.0	%
		Contrast = 7Fh				
		Contrast = 3Fh				

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CS}	Icon Segment Output Current Setting: Icon Current Range = FFh, Individual Icon Current = 7Fh for all 64 icons (Icon segment pins under test is connected with a 20KΩ resistive load to V_{SS})	Display OFF, No panel attached	-5	0	+5	uA
		Display ON, No panel attached	117	130	143	uA
Icon Dev	Icon Segment Output Current Uniformity $Dev = (I_{SEG} – I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ $I_{SEG}[0:127]$ = Segment current at particular contrast setting	Contrast = FFh	-	-	±3	%
Icon Adj. Dev	Adjacent pin output current uniformity	Adj Dev = (I[n] - I[n+1]) / (I[n]+I[n+1])	-	±2.0	-	%
R_{COM_ON}	COM pin output resistance	COM[0:127]	-	25	30	Ω

13 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
$V_{DD} = V_{DDIO} = 2.4V$ to $3.5V$
$V_{CC} = 9.0V$ to $16.0V$
$T_A = 25°C$

Table 13-1: AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.8V$	450	500	550	KHz
F_{FRM}	Frame Frequency	Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1 / (D x K x N)	-	Hz
RES#	Reset low pulse width	-	3	-	-	us
	Reset completion time	-	-	-	2	us

Note:

(1) Fosc stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.
(2) D stands for divide ratio
(3) K stands for total number of display clocks per row defined by command B2h
(4) N stands for number of MUX selected by command A8h

Conditions:

V_{DD} ~ V_{SS} = 2.4 to 3.5V

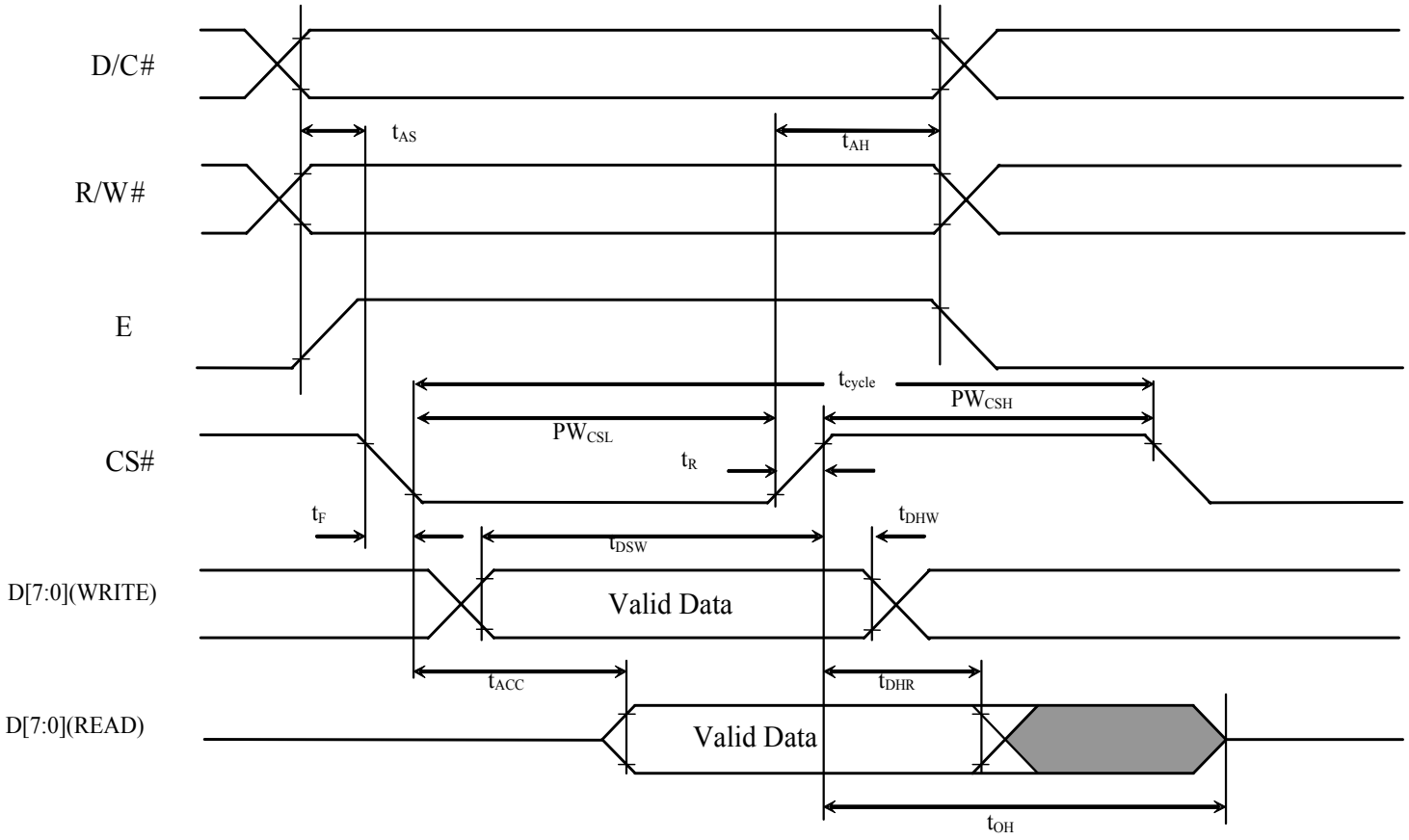
V_{DDIO} = V_{DD}

T_A = 25°C

Table 13-2: 6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1: 6800-series MPU parallel interface characteristics



Conditions:

V_{DD} ~ V_{SS} = 2.4 to 3.5V

$V_{DDIO} = V_{DD}$

T_A = 25°C

Table 13-3: 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics (Form 1)

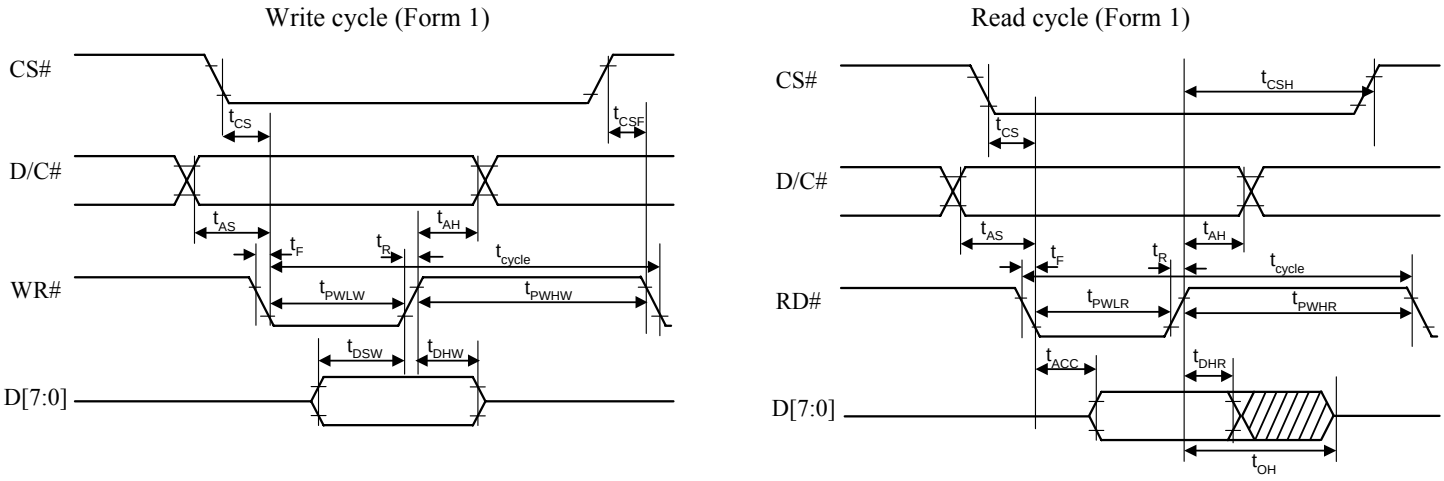
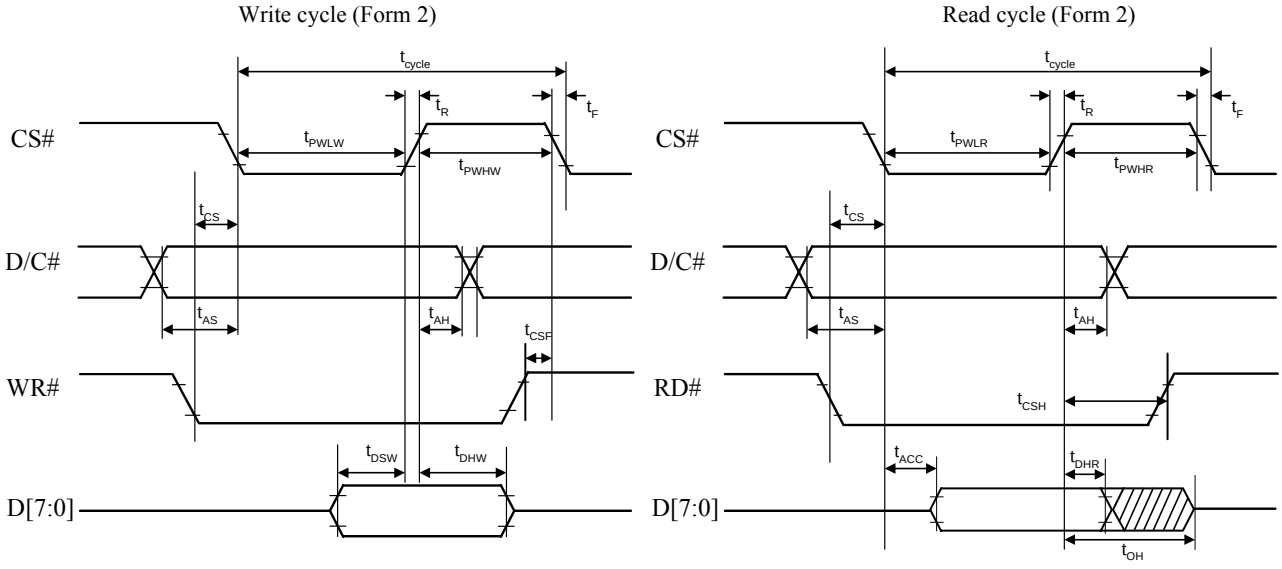


Figure 13-3 : 8080-series parallel interface characteristics (Form 2)



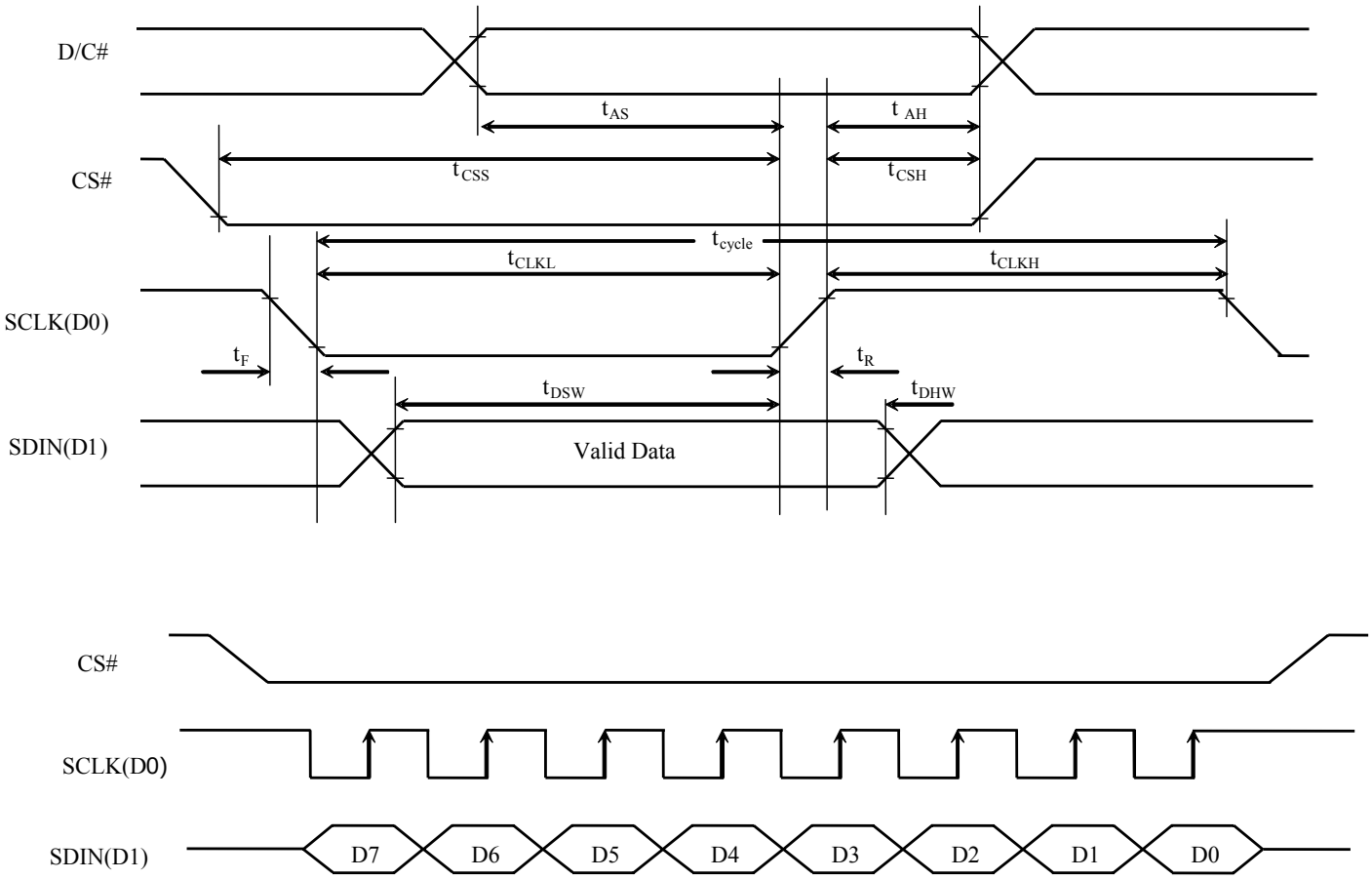
Conditions:

V_{DD} ~ V_{SS} = 2.4 to 3.5V
$V_{DDIO} = V_{DD}$
T_A = 25°C

Table 13-4: Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

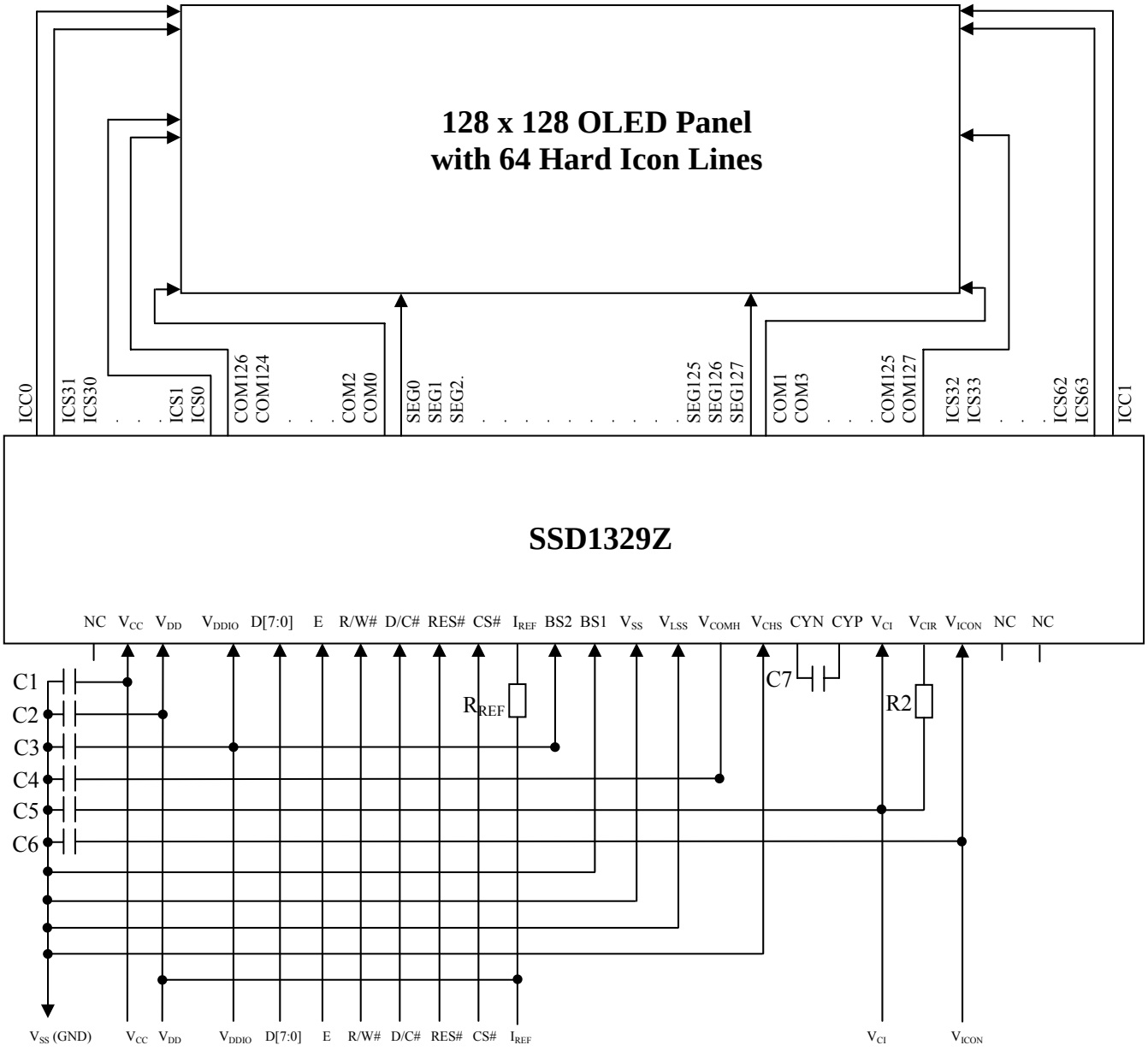
Figure 13-4: Serial interface characteristics



14 APPLICATION EXAMPLES

Figure 14-1: Application Example for SSD1329 8-bit 6800-parallel interface mode

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{DD} 2.7V, V_{DDIO} = 1.8V, V_{CC} = 11.0V, V_{CI} = 3.5V, I_{REF} = 10uA)



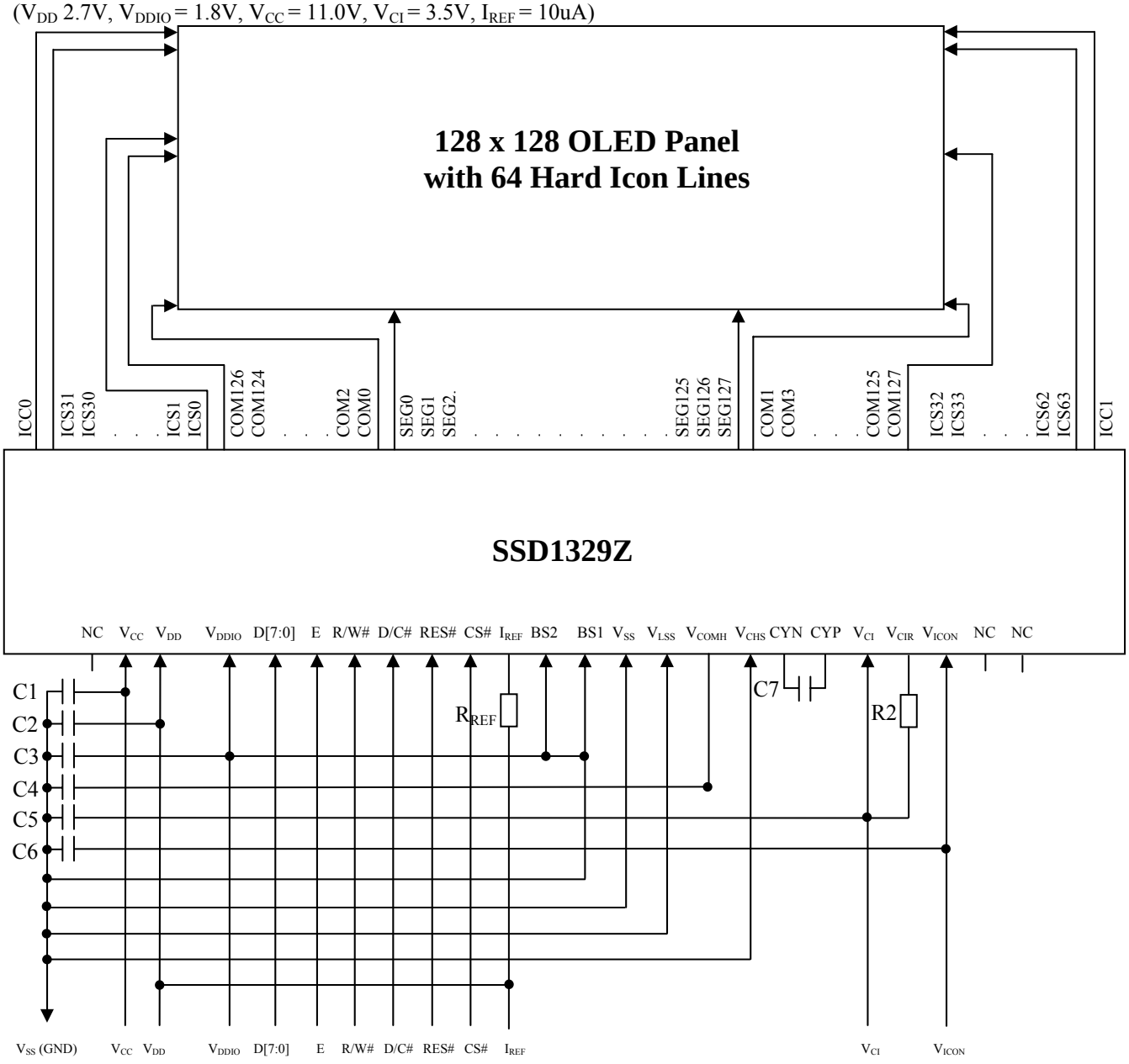
Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, RES#, CS#
Pin internally connected to V_{DDIO}: CLS
Pin externally connected to V_{DDIO}: BS2
Pin externally connected to V_{SS}: V_{LSS} , V_{CHS} , BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C1 ~ C5 and C7: 1uF in which C1, C4 have to be tantalum capacitors (1)
C6: 2uF in which C6 has to be tantalum capacitor (1)
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / IREF = (3.00 – 1.00)V / 10uA = 200K Ω
R2 = 33 Ω

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

Figure 14-2: Application Example for SSD1329 8-bit 8080-parallel interface mode

The configuration for 8-bit 8080-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{DD} 2.7V, V_{DDIO} = 1.8V, V_{CC} = 11.0V, V_{CI} = 3.5V, I_{REF} = 10uA)



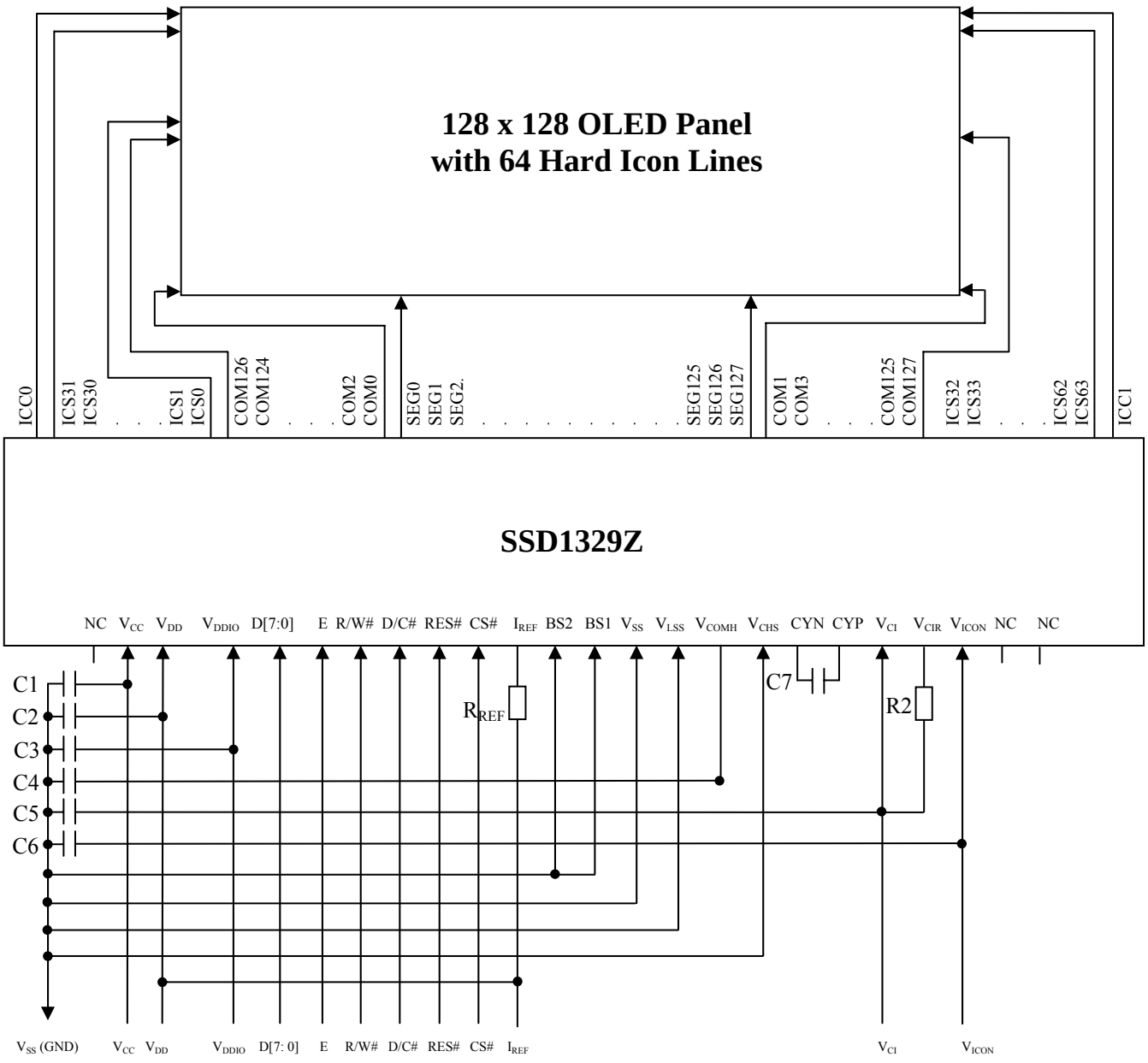
Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, RES#, CS#
Pin internally connected to V_{DDIO}: CLS
Pin externally connected to V_{DDIO}: BS2
Pin externally connected to V_{SS}: V_{LSS}, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C1 ~ C5 and C7: 1uF in which C1, C4 have to be tantalum capacitors (1)
C6: 2uF in which C6 has to be tantalum capacitor (1)
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R2 = 33Ω

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

Figure 14-3: Application Example for SSD1329 8-bit SPI-serial interface mode

The configuration for SPI-serial interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} 2.7V, V_{DDIO} = 1.8V, V_{CC} = 11.0V, V_{CI} = 3.5V, I_{REF} = 10uA)



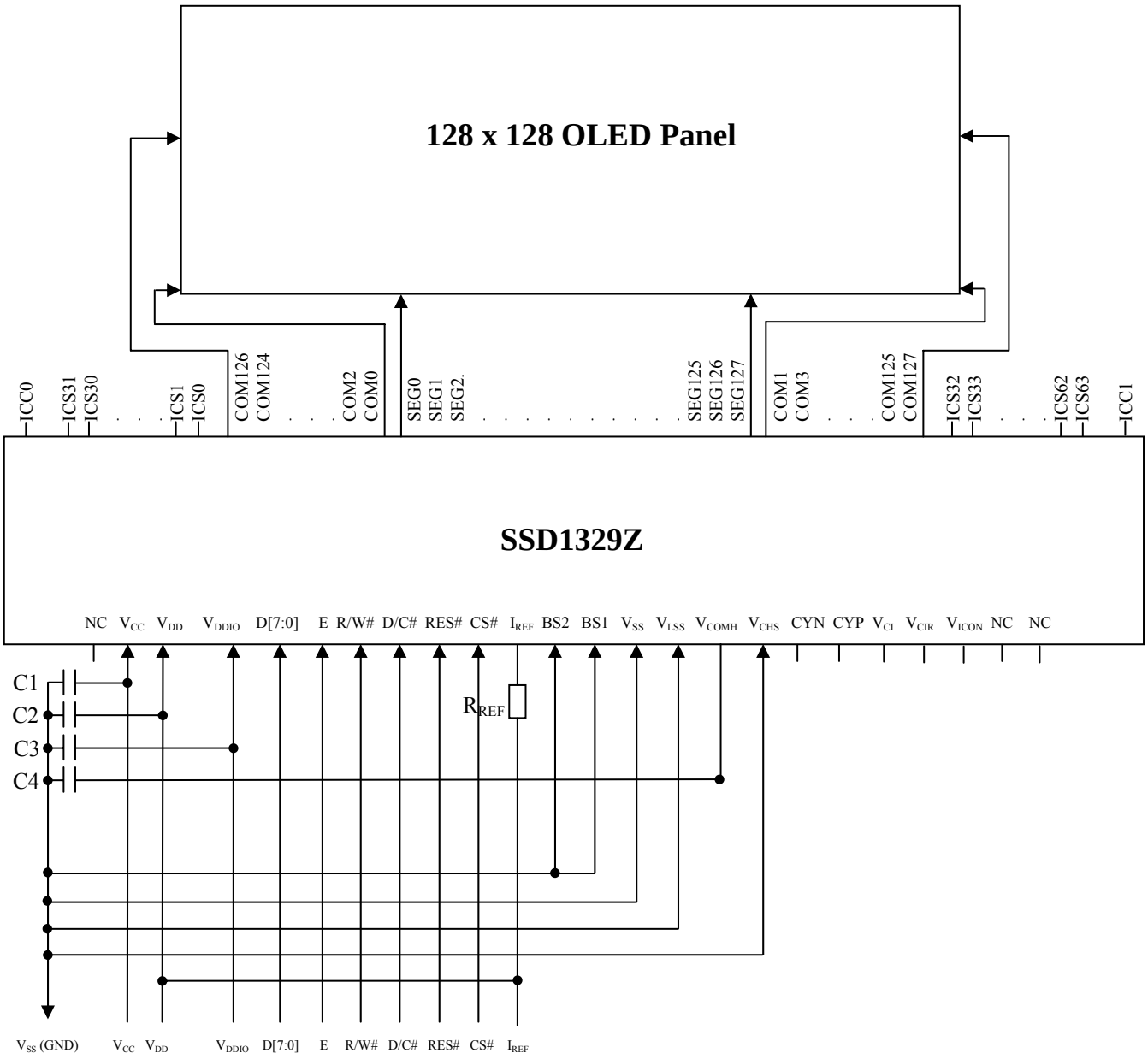
Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, RES#, CS#
Pin internally connected to V_{DDIO}: CLS
Pin externally connected to V_{DDIO}: BS2
Pin externally connected to V_{SS}: V_{LSS}, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C1 ~ C5 and C7: 1uF in which C1, C4 have to be tantalum capacitors (1)
C6: 2uF in which C6 has to be tantalum capacitor (1)
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R2 = 33Ω

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

Figure 14-4: Application Example for SSD1329 when hard icons are not used.

The configuration for SPI-serial interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} 2.7V, V_{DDIO} = 1.8V, V_{CC} = 11.0V, I_{REF} = 10uA)



Pin connected to MCU interface: D[7:0], E, R/W#, D/C#, RES#, CS#
Pin internally connected to V_{DDIO}: CLS
Pin externally connected to V_{DDIO}: BS2
Pin externally connected to V_{SS}: V_{LSS}, V_{CHS}, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

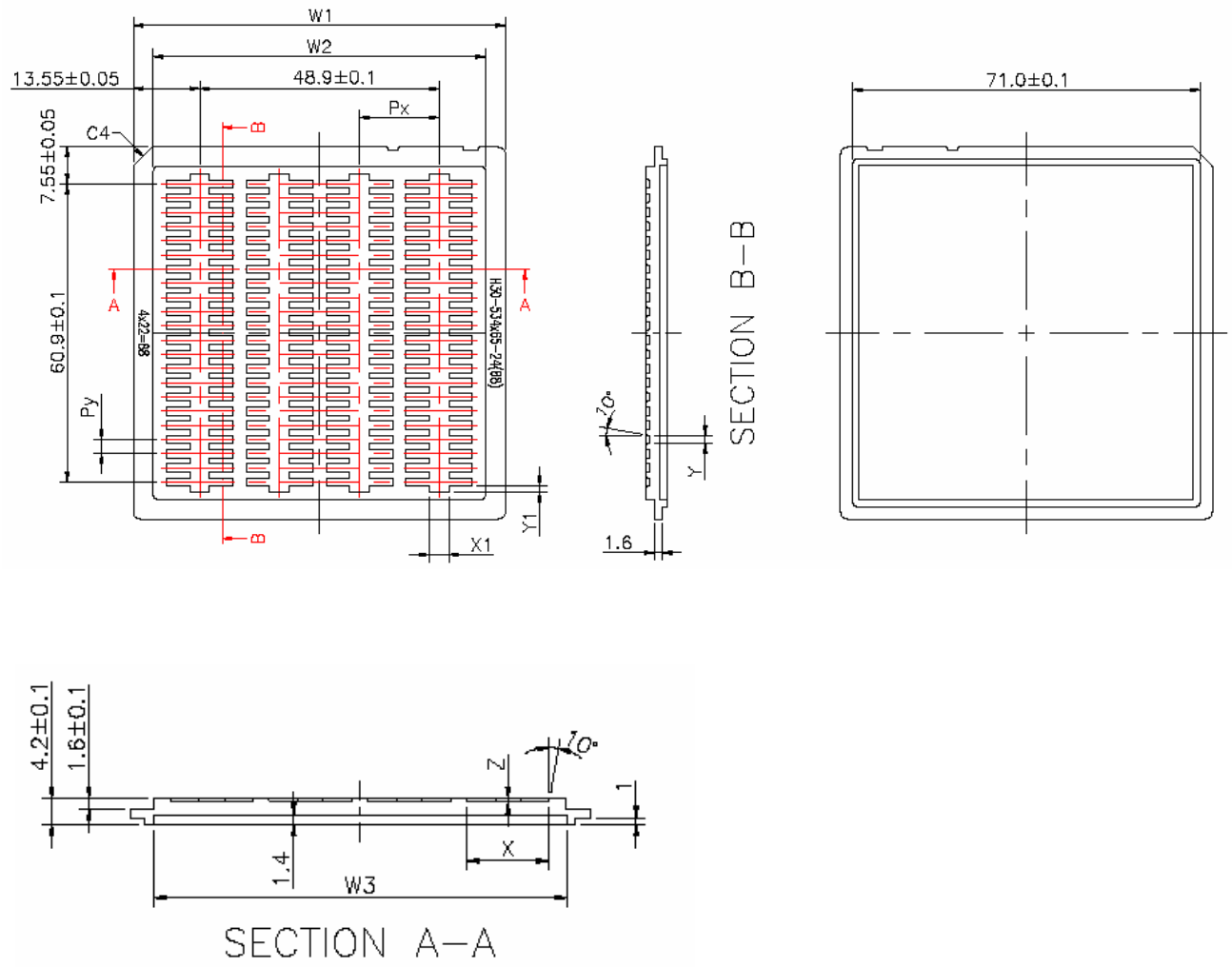
C1 ~ C4: 1uF in which C1, C4 have to be tantalum capacitors [(1)]
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R2 = 33 Ω

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

15.1 SSD1329Z Die Tray Information

Figure 15-1: Die Tray Information



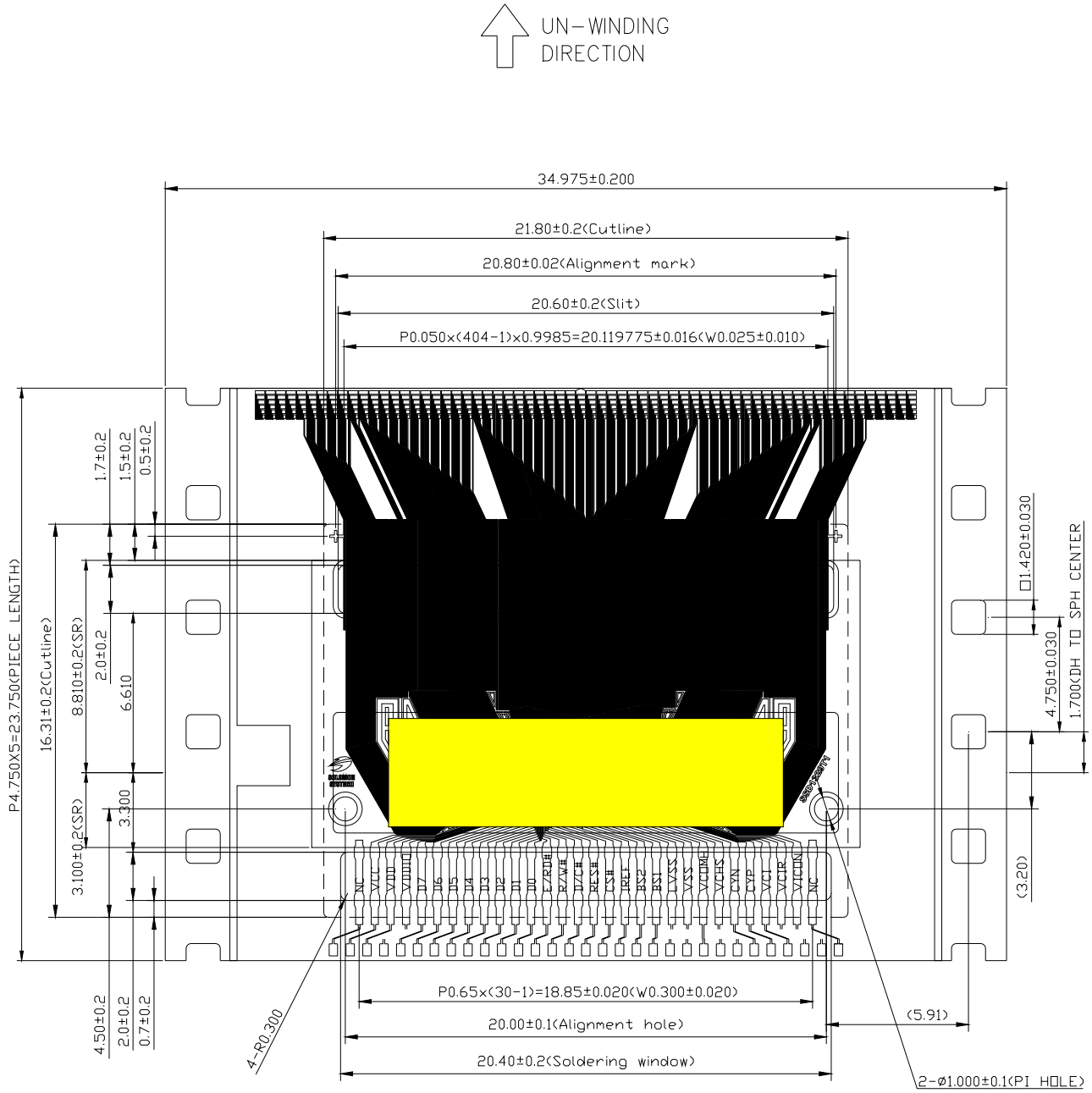
	Spec	
	mm	(mil)
W1	76.00 ± 0.1	(2992)
W2	68.00 ± 0.1	(2677)
W3	68.30 ± 0.1	(2689)
X1	4.00 ± 0.1	(157)
Y1	1.25 ± 0.1	(49)
Px	16.30 ± 0.05	(642)
Py	2.90 ± 0.05	(114)
X	13.56 ± 0.05	(534)
Y	1.65 ± 0.05	(65)
Z	0.61 ± 0.05	(24)
N	88	

Remark

1. Depth of text: Max. 0.1mm
2. Tray material: ABS
3. Tray color code: Black
4. Surface resistance $10^9 \sim 10^{11}$ Ω
5. Tray warpage: Max 0.10mm
6. Unspecifier dim's tolerance: ± 0.15mm
7. Pocket size: 13.56 x 1.65 x 0.61mm

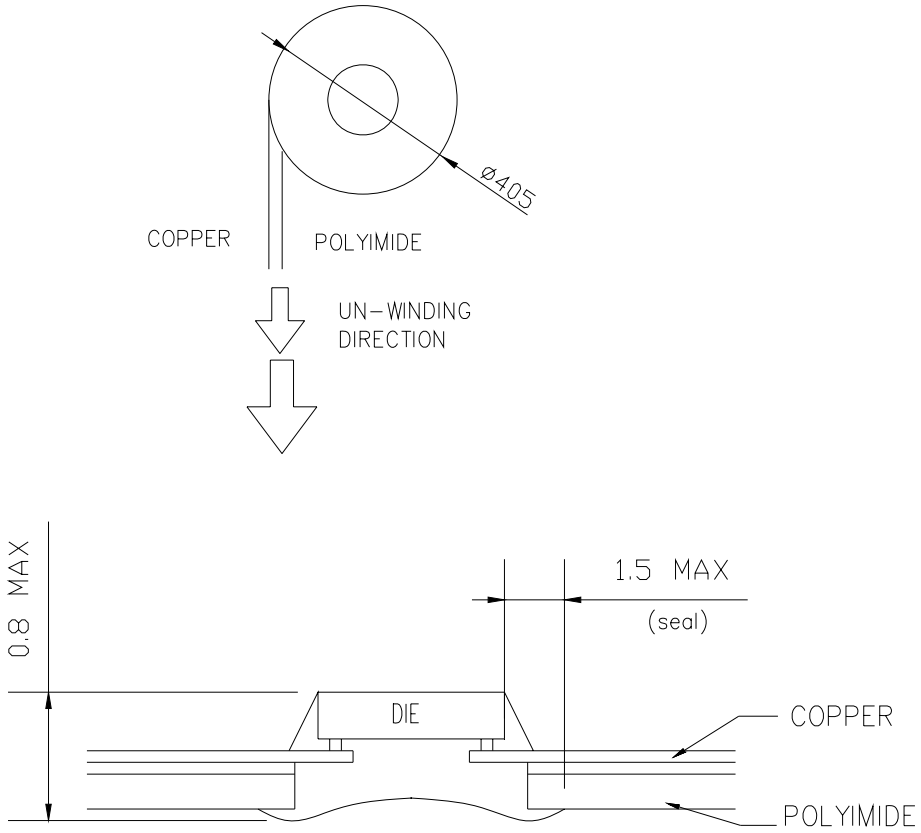
15.2 SSD1329T1R1 Detail Dimension

Figure 15-2: SSD1329T1R1 detail dimension



NOTE:

1. MATERIAL
   PI: 75±8um
   ADHESIVE: 12±3um
   CU: 18±5um
   SR: 26±14um;TOLERANCE±0.200mm
   FLEX COATING: Min10um
2. SN PLATING: 0.210±0.05um
3. TAPESITE: 5 SPH, 23.75mm



MIRROR DESIGN

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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