



NOVATEK
聯詠科技

Data Sheet

NT39411

TFT LCD Source Driver

V0.6

Preliminary Spec

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Revise History

NT39411 Specification Revision History			
Version	Content	Page	Date
0.6	Modify DIO1/DIO2 description	7	2007/8/17
0.5	Revise Timing Diagram 1.2 TTL mode	17	2006/7/24
	Revise DC Electrical Characteristics	14	2006/8/25
	Revise Document Format	All	2006/8/30
0.4	Modify Features and General Description	4	2006/7/11
	Add Pin and Pad Descriptions "CLKN"	7	
	Modify Pin and Pad Description "CHNSL", "CHNDS"	8	2006/7/12
	Modify Output Voltage VS Input Data	11,12	
	Modify DC Electrical Characteristics	13,14	
0.3	Revise all	All	2006/6/13
0.2	Revise Pin Assignment	5	2006/4/14
	Chip Outline Dimension (Bump size)	16	
	Align Mark and Dimension Table	17	
	Block Diagram	6	
0.1	New Release	-	2006/4/12

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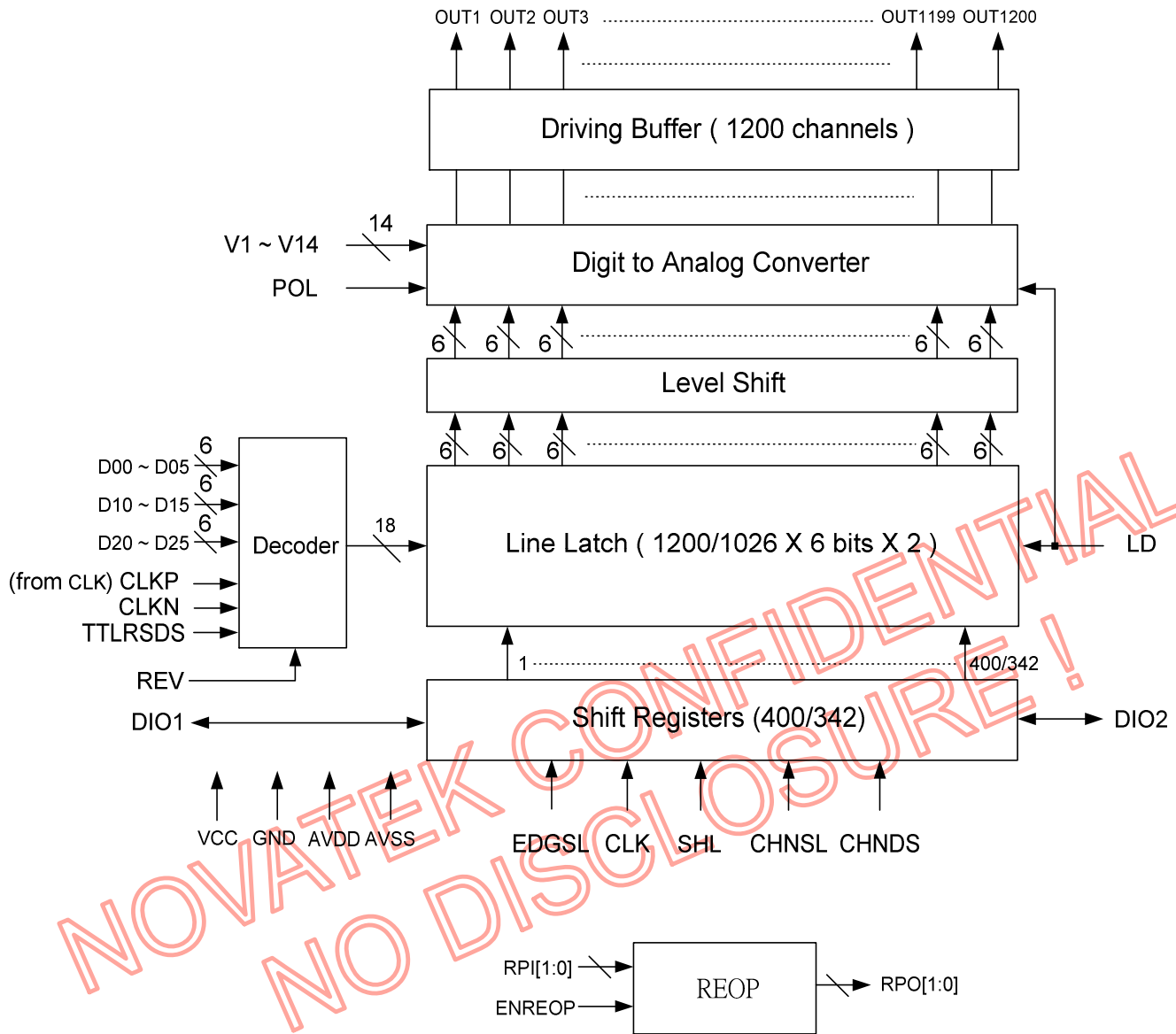
Features

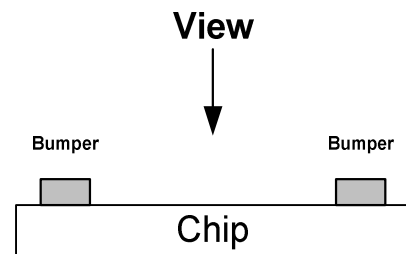
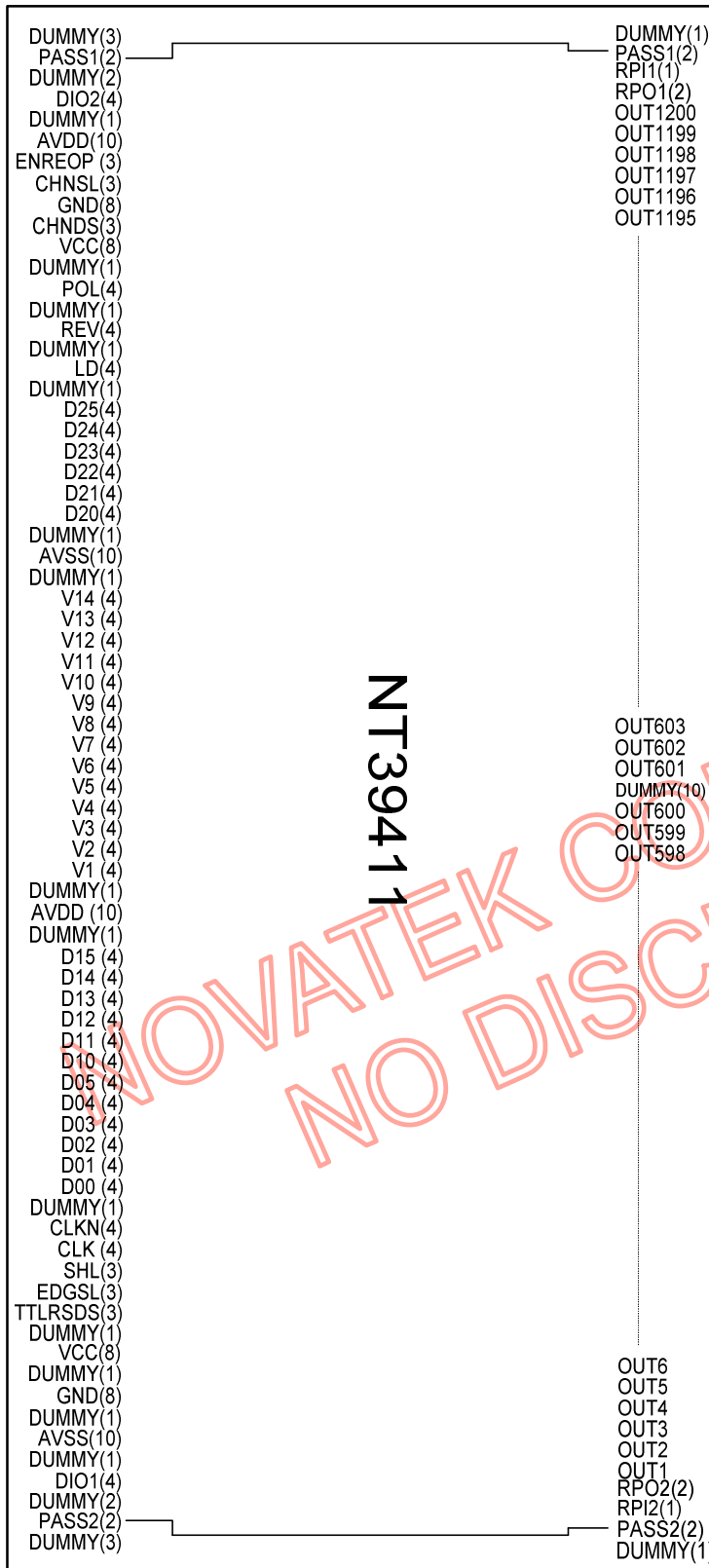
- Output: 1200/1026 output channels
- 6-bit resolution / 64 gray scale
- Dot inversion with polarity control
- V1 ~ V14 for adjusting Gamma correction
- Power of LCD driving voltage: 6.5 ~ 13.5V
- Output dynamic range: 0.1 ~ AVDD-0.1V
- Power consumption of analog circuit: 12mA
- Power for interface circuit: 2.7 ~ 3.6V
- Operating frequency: 50 MHz
- Output deviation: $\pm 20\text{mV}$
- Data inverting for reducing EMI
- Cascade function with bi-direction shift control
- Build in 2 repair OP
- CMOS silicon gate (p-type substrate)
- COG package

General Description

NT39411 is a 1200/1026 channel data driver IC with TTL/RSDS interface for color TFT LCD panels . For lower power dissipation , the circuit architecture with a special method is designed , and dot inversion is suggested on application. For better performance, a wide range of supply voltages and small output deviations are designed in this chip. This chip also supplies 14 sections of voltage-reference select for gamma correction. And the power dissipation on the gamma correction resistors is also concerned, making this chip more suitable for mid or small sized color TFT panels.

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Function Block Diagram


Pad Sequence (Bump Side)


Pad Description

Designation	I/O	Description																					
Input signal																							
D05 ~ D00 D15 ~ D10 D25 ~ D20	I	<p>These pins can be used as TTL or RSDS data input by TTLRSDS pin setting. For RSDS input mode, the 3-bit differential input pairs generate the internal 6-bit data through the comparison between DxxP and DxxN. For TTL input mode as D00 ~ D05, D10 ~ D15, D20 ~ D25 input pin.</p> <table border="1"> <thead> <tr> <th>Pin name</th> <th>RSDS input mode TTLRSDS = H</th> <th>TTL input mode TTLRSDS = L</th> </tr> </thead> <tbody> <tr> <td>D04 , D02 , D00</td> <td>D0[2:0]N</td> <td>D04 , D02 , D00</td> </tr> <tr> <td>D05 , D03 , D01</td> <td>D0[2:0]P</td> <td>D05 , D03 , D01</td> </tr> <tr> <td>D14 , D12 , D10</td> <td>D1[2:0]N</td> <td>D14 , D12 , D10</td> </tr> <tr> <td>D15 , D13 , D11</td> <td>D1[2:0]P</td> <td>D15 , D13 , D11</td> </tr> <tr> <td>D24 , D22 , D20</td> <td>D2[2:0]N</td> <td>D24 , D22 , D20</td> </tr> <tr> <td>D25 , D23 , D21</td> <td>D2[2:0]P</td> <td>D25 , D23 , D21</td> </tr> </tbody> </table>	Pin name	RSDS input mode TTLRSDS = H	TTL input mode TTLRSDS = L	D04 , D02 , D00	D0[2:0]N	D04 , D02 , D00	D05 , D03 , D01	D0[2:0]P	D05 , D03 , D01	D14 , D12 , D10	D1[2:0]N	D14 , D12 , D10	D15 , D13 , D11	D1[2:0]P	D15 , D13 , D11	D24 , D22 , D20	D2[2:0]N	D24 , D22 , D20	D25 , D23 , D21	D2[2:0]P	D25 , D23 , D21
Pin name	RSDS input mode TTLRSDS = H	TTL input mode TTLRSDS = L																					
D04 , D02 , D00	D0[2:0]N	D04 , D02 , D00																					
D05 , D03 , D01	D0[2:0]P	D05 , D03 , D01																					
D14 , D12 , D10	D1[2:0]N	D14 , D12 , D10																					
D15 , D13 , D11	D1[2:0]P	D15 , D13 , D11																					
D24 , D22 , D20	D2[2:0]N	D24 , D22 , D20																					
D25 , D23 , D21	D2[2:0]P	D25 , D23 , D21																					
REV	I	Controls whether the data of D00~D25 are inverted or not, normally pulled low. When "REV"=1 these data will be inverted. EX. "00" → "3F", "07" → "38", "15" → "2A", and so on.																					
CLK	I	Clock input. When RSDS input mode, CLK is used as CLKP input pin. Latching source data onto the line latches at the rising or falling edge by EDGSL signal selected.																					
CLKN	I	The RSDS clock input pairs generate the internal shift clock through the comparison between CLKP and CLKN. When TTL mode , tie to GND.																					
V1 ~ V14	I	Gamma correction reference voltage. The voltage of these pins must be AVSS<V14<V13<V12<V11<V10<V9< V8; V7< V6<V5<V4<V3<V2<V1< AVDD																					
SHL	I	<p>Select left or right shift, normally pulled high.</p> <p>SHL="1" : DIO1 → OUT1,2,3 → OUT4,5,6 →→ OUT1198,1199,1200 = DIO2</p> <p>SHL="0" : DIO1= OUT1,2,3 ←← OUT4,5,6 ←← OUT1198,1199,1200 ← DIO2</p> <table border="1"> <thead> <tr> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> <th>SHIFT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Input</td> <td>Output</td> <td>Right</td> </tr> <tr> <td>0</td> <td>Output</td> <td>Input</td> <td>Left</td> </tr> </tbody> </table>	SHL	DIO1	DIO2	SHIFT	1	Input	Output	Right	0	Output	Input	Left									
SHL	DIO1	DIO2	SHIFT																				
1	Input	Output	Right																				
0	Output	Input	Left																				
DIO1 DIO2	I/O	<p>Start pulse signal input/output.</p> <p>When SHL is applied high (SHL="1"), a start high-pulse on DIO1 is latched at the rising edge of the CLK. Then the data are latched serially onto internal latches at the rising or falling edge of the CLK. After all line latches are full with data, 340/342/400 or 170/171/200 clocks, a pulse is shifted out through the DIO2 pin at the rising edge of the CLK. This function can cascade two or more devices for dot-size expansion. In normal applications, the DIO2 signal of the first device is connected to the DIO1 of the second stage, and the DIO2 of the second one is connected to the DIO1 of the third, and so on like a daisy chain. In contrast , when SHL is applied low, a start pulse inputs on DIO2, and a pulse outputs through DIO1.</p> <p>*Remark: The input pulse-width of DIO1/2 may be over 1 clock-cycle.</p>																					
EDGSL	I	<p>Clock edge selected, normally pulled low.</p> <p>When EDGSL= "0", Latching source data onto the line latches at the rising edge.</p> <p>When EDGSL= "1", Latching source data onto the line latches at the rising edge and falling edge.</p> <p>*Remark: Please reference Timing Diagram 2.1 Clock and data input timing diagram 1.</p>																					

LD	I	Latches the polarity of outputs and switches the new data to outputs. 1. At the rising edge, latches the "POL" signal to control the polarity of the outputs. 2. The pin also controls the switch of the line registers that switches the new incoming data to outputs. *Remark: The LD may switch the new data to outputs at any time even if the line data are not completely full.															
POL	I	Polarity selector for the dot-inversion control. Available at the rising edge of LD. "POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs. "POL=1" represents that even outputs are of positive polarity with a voltage ranging from V1 to V7, and odd outputs are of negative polarity with a voltage ranging from V8 to V14. On the other hand, if LD has low level "POL", even outputs are of negative polarity and odd outputs are of positive. POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14 POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7															
ENREOP	I	ENREOP = H : Enable repair line OP RPI1/2 , RPO1/2. ENREOP = L or open : Disable repair line OP RPI1/2 , RPO1/2. (default ENREOP = L)															
TTLRSDS	I	TTLRSDS = H : RSDS data input TTLRSDS = L or open : TTL data input (default TTLRSDS = L)															
CHNSL	I	Output channel selection , default CHNSL = H, <table border="1" data-bbox="560 892 1425 997"> <thead> <tr> <th>CHNSL</th> <th>Output channel</th> <th>Disable channel</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>1200</td> <td>none</td> </tr> <tr> <td>L</td> <td>1026(CHNDS = L)</td> <td>OUT514 ~ OUT687</td> </tr> </tbody> </table>	CHNSL	Output channel	Disable channel	H	1200	none	L	1026(CHNDS = L)	OUT514 ~ OUT687						
CHNSL	Output channel	Disable channel															
H	1200	none															
L	1026(CHNDS = L)	OUT514 ~ OUT687															
CHNDS	I	Additional disable channel selection for 1026 channel mode only, default CHNDS = L(none additional disable channel). <table border="1" data-bbox="560 1066 1463 1241"> <thead> <tr> <th>CHNSL</th> <th>CHNDS</th> <th>Output channel</th> <th>Disable channel</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>L</td> <td>1200</td> <td>none</td> </tr> <tr> <td rowspan="2">L</td> <td>L</td> <td>1026</td> <td>OUT514 ~ OUT687</td> </tr> <tr> <td>H</td> <td>1020</td> <td>OUT514 ~ OUT687, OUT1195 ~ OUT1200</td> </tr> </tbody> </table> <p>Note : CHNSL = "H" and CHNDS = "H" is inhibited.</p>	CHNSL	CHNDS	Output channel	Disable channel	H	L	1200	none	L	L	1026	OUT514 ~ OUT687	H	1020	OUT514 ~ OUT687, OUT1195 ~ OUT1200
CHNSL	CHNDS	Output channel	Disable channel														
H	L	1200	none														
L	L	1026	OUT514 ~ OUT687														
	H	1020	OUT514 ~ OUT687, OUT1195 ~ OUT1200														
Power																	
AVDD	PI	Power supply for analog circuits															
AVSS	PI	Ground pins for analog circuits															
VCC	PI	Power supply for digital circuits															
GND	PI	Ground pins for digital circuits															
Others																	
OUT1 ~OUT1200	O	Output driver signals.															
RPO1,RPO2	O	RPI1 (RPI2) → impedance changed → RPO1 (RPO2)															
DUMMY0 ~ DUMMY35	D	Dummy pads. Not connected															

I: Input, O: Output, D: Dummy, PI: Power input, I/O: Input / Output.

Pass line name:

PASS LINE NO.	PIN NAME	PIN NAME
1	PASS1	PASS1
2	PASS2	PASS2

Function Description

1. Power on/off sequence

This IC is a high-voltage LCD driver, so may be damaged by a large current flow when an incorrect power sequence is used. The recommended sequence should be : digital power (VCC&GND) → logic signals → analog power (AVDD&AVSS) → Gamma correction reference voltage(V1~V14). Reverse this sequence to shut down, or turn off all signals and power simultaneously.

2. RSDS Receiver and Demultiplexer

The device adapts the RSDS interface for EMI solution. The internal RSDS receiver block operates the comparison between the transmitted differential input pair data. The input data line from the timing controller to the RSDS receiver consist of 6-bit digital , 3 color, 1 port, 9 differential data pair (DxxP/DxxN) and 1 differential clock pair(CLKP/CLKN). The input common mode voltage range at the RSDS receiver is 1.2V. The differential data and clock signals from the panel timing controller arrive at the NT39411 as multi-plexed , even and odd data fields. The nominal peak to peak swing of the data is 200mV across a termination resistor.

3. Relationship between the order of input data and output channels

(1) SHL="1", shift right, a start pulse from DIO1

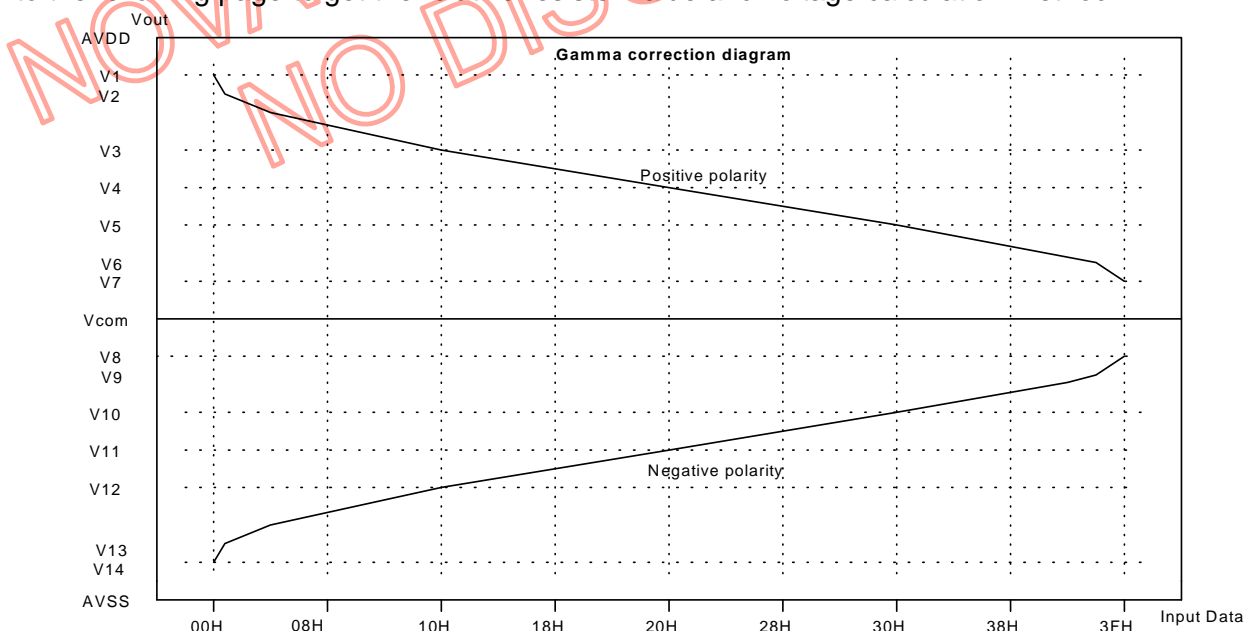
Output	OUT1	OUT2	OUT3	---	OUT1198	OUT1199	OUT1200
Order	First data			---→	Last data		
Data	D05~D00	D15~D10	D25~D20	---	D05~D00	D15~D10	D25~D20

(2) SHL="0", shift left, a start pulse from DIO2

Output	OUT1	OUT2	OUT3	---	OUT1198	OUT1199	OUT1200
Order	Last data			←---	First data		
Data	D05~D00	D15~D10	D25~D20	---	D05~D00	D15~D10	D25~D20

4. Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage with the polarity. The range of V1~ V7 is for positive polarity, and V8 ~ V14 for negative polarity. Please refer to the following page to get the relative resistor value and voltage calculation method.



Remark: AVDD-0.1 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ V6 ≥ V7; V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ V14 ≥ AVSS+0.1V

5. Gamma correction resistor ratio

	Name	Resistor	Name	Resistor	
V1, V14 →	R0	6.4	R32	0.8	← V4, V11
V2, V13 →	R1	6	R33	0.8	
	R2	5.6	R34	0.8	
	R3	5.2	R35	0.8	
	R4	4.8	R36	0.8	
	R5	4.4	R37	0.8	
	R6	4.4	R38	0.8	
	R7	4	R39	0.8	
	R8	4	R40	0.8	
	R9	3.2	R41	0.8	
	R10	3.2	R42	0.8	
	R11	2.8	R43	0.8	
	R12	2.8	R44	0.8	
	R13	2.8	R45	0.8	
	R14	2.4	R46	0.8	
	R15	2.4	R47	0.8	
V3, V12 →	R16	2.4	R48	0.8	← V5, V10
	R17	2	R49	0.8	
	R18	2	R50	0.8	
	R19	2	R51	0.8	
	R20	1.6	R52	0.8	
	R21	1.6	R53	1.2	
	R22	1.6	R54	1.2	
	R23	1.2	R55	1.2	
	R24	1.2	R56	1.6	
	R25	1.2	R57	1.6	
	R26	1.2	R58	2	
	R27	0.8	R59	2	
	R28	0.8	R60	2.4	
	R29	0.8	R61	4	← V6, V9
	R30	0.8	R62	6.4	← V7, V8
V4, V11 →	R31	0.8			

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6. Output Voltage VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	V2	V13
02H	$V3 + (V2 - V3)X$ 52 / 58	$V13 + (V12 - V13)X$ 6 / 58
03H	$V3 + (V2 - V3)X$ 46.4 / 58	$V13 + (V12 - V13)X$ 11.6 / 58
04H	$V3 + (V2 - V3)X$ 41.2 / 58	$V13 + (V12 - V13)X$ 16.8 / 58
05H	$V3 + (V2 - V3)X$ 36.4 / 58	$V13 + (V12 - V13)X$ 21.6 / 58
06H	$V3 + (V2 - V3)X$ 32 / 58	$V13 + (V12 - V13)X$ 26 / 58
07H	$V3 + (V2 - V3)X$ 27.6 / 58	$V13 + (V12 - V13)X$ 30.4 / 58
08H	$V3 + (V2 - V3)X$ 23.6 / 58	$V13 + (V12 - V13)X$ 34.4 / 58
09H	$V3 + (V2 - V3)X$ 19.6 / 58	$V13 + (V12 - V13)X$ 38.4 / 58
0AH	$V3 + (V2 - V3)X$ 16.4 / 58	$V13 + (V12 - V13)X$ 41.6 / 58
0BH	$V3 + (V2 - V3)X$ 13.2 / 58	$V13 + (V12 - V13)X$ 44.8 / 58
0CH	$V3 + (V2 - V3)X$ 10.4 / 58	$V13 + (V12 - V13)X$ 47.6 / 58
0DH	$V3 + (V2 - V3)X$ 7.6 / 58	$V13 + (V12 - V13)X$ 50.4 / 58
0EH	$V3 + (V2 - V3)X$ 4.8 / 58	$V13 + (V12 - V13)X$ 53.2 / 58
0FH	$V3 + (V2 - V3)X$ 2.4 / 58	$V13 + (V12 - V13)X$ 55.6 / 58
10H	V3	V12
11H	$V4 + (V3 - V4)X$ 19.6 / 22	$V12 + (V11 - V12)X$ 2.4 / 22
12H	$V4 + (V3 - V4)X$ 17.6 / 22	$V12 + (V11 - V12)X$ 4.4 / 22
13H	$V4 + (V3 - V4)X$ 15.6 / 22	$V12 + (V11 - V12)X$ 6.4 / 22
14H	$V4 + (V3 - V4)X$ 13.6 / 22	$V12 + (V11 - V12)X$ 8.4 / 22
15H	$V4 + (V3 - V4)X$ 12 / 22	$V12 + (V11 - V12)X$ 10 / 22
16H	$V4 + (V3 - V4)X$ 10.4 / 22	$V12 + (V11 - V12)X$ 11.6 / 22
17H	$V4 + (V3 - V4)X$ 8.8 / 22	$V12 + (V11 - V12)X$ 13.2 / 22
18H	$V4 + (V3 - V4)X$ 7.6 / 22	$V12 + (V11 - V12)X$ 14.4 / 22
19H	$V4 + (V3 - V4)X$ 6.4 / 22	$V12 + (V11 - V12)X$ 15.6 / 22
1AH	$V4 + (V3 - V4)X$ 5.2 / 22	$V12 + (V11 - V12)X$ 16.8 / 22
1BH	$V4 + (V3 - V4)X$ 4 / 22	$V12 + (V11 - V12)X$ 18 / 22
1CH	$V4 + (V3 - V4)X$ 3.2 / 22	$V12 + (V11 - V12)X$ 18.8 / 22
1DH	$V4 + (V3 - V4)X$ 2.4 / 22	$V12 + (V11 - V12)X$ 19.6 / 22
1EH	$V4 + (V3 - V4)X$ 1.6 / 22	$V12 + (V11 - V12)X$ 20.4 / 22
1FH	$V4 + (V3 - V4)X$ 0.8 / 22	$V12 + (V11 - V12)X$ 21.2 / 22

(continued)

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	$V5 + (V4 - V5) \times 12 / 12.8$	$V11 + (V10 - V11) \times 0.8 / 12.8$
22H	$V5 + (V4 - V5) \times 11.2 / 12.8$	$V11 + (V10 - V11) \times 1.6 / 12.8$
23H	$V5 + (V4 - V5) \times 10.4 / 12.8$	$V11 + (V10 - V11) \times 2.4 / 12.8$
24H	$V5 + (V4 - V5) \times 9.6 / 12.8$	$V11 + (V10 - V11) \times 3.2 / 12.8$
25H	$V5 + (V4 - V5) \times 8.8 / 12.8$	$V11 + (V10 - V11) \times 4 / 12.8$
26H	$V5 + (V4 - V5) \times 8 / 12.8$	$V11 + (V10 - V11) \times 4.8 / 12.8$
27H	$V5 + (V4 - V5) \times 7.2 / 12.8$	$V11 + (V10 - V11) \times 5.6 / 12.8$
28H	$V5 + (V4 - V5) \times 6.4 / 12.8$	$V11 + (V10 - V11) \times 6.4 / 12.8$
29H	$V5 + (V4 - V5) \times 5.6 / 12.8$	$V11 + (V10 - V11) \times 7.2 / 12.8$
2AH	$V5 + (V4 - V5) \times 4.8 / 12.8$	$V11 + (V10 - V11) \times 8 / 12.8$
2BH	$V5 + (V4 - V5) \times 4 / 12.8$	$V11 + (V10 - V11) \times 8.8 / 12.8$
2CH	$V5 + (V4 - V5) \times 3.2 / 12.8$	$V11 + (V10 - V11) \times 9.6 / 12.8$
2DH	$V5 + (V4 - V5) \times 2.4 / 12.8$	$V11 + (V10 - V11) \times 10.4 / 12.8$
2EH	$V5 + (V4 - V5) \times 1.6 / 12.8$	$V11 + (V10 - V11) \times 11.2 / 12.8$
2FH	$V5 + (V4 - V5) \times 0.8 / 12.8$	$V11 + (V10 - V11) \times 12 / 12.8$
30H	V5	V10
31H	$V6 + (V5 - V6) \times 20.4 / 21.2$	$V10 + (V9 - V10) \times 0.8 / 21.2$
32H	$V6 + (V5 - V6) \times 19.6 / 21.2$	$V10 + (V9 - V10) \times 1.6 / 21.2$
33H	$V6 + (V5 - V6) \times 18.8 / 21.2$	$V10 + (V9 - V10) \times 2.4 / 21.2$
34H	$V6 + (V5 - V6) \times 18 / 21.2$	$V10 + (V9 - V10) \times 3.2 / 21.2$
35H	$V6 + (V5 - V6) \times 17.2 / 21.2$	$V10 + (V9 - V10) \times 4 / 21.2$
36H	$V6 + (V5 - V6) \times 16 / 21.2$	$V10 + (V9 - V10) \times 5.2 / 21.2$
37H	$V6 + (V5 - V6) \times 14.8 / 21.2$	$V10 + (V9 - V10) \times 6.4 / 21.2$
38H	$V6 + (V5 - V6) \times 13.6 / 21.2$	$V10 + (V9 - V10) \times 7.6 / 21.2$
39H	$V6 + (V5 - V6) \times 12 / 21.2$	$V10 + (V9 - V10) \times 9.2 / 21.2$
3AH	$V6 + (V5 - V6) \times 10.4 / 21.2$	$V10 + (V9 - V10) \times 10.8 / 21.2$
3BH	$V6 + (V5 - V6) \times 8.4 / 21.2$	$V10 + (V9 - V10) \times 12.8 / 21.2$
3CH	$V6 + (V5 - V6) \times 6.4 / 21.2$	$V10 + (V9 - V10) \times 14.8 / 21.2$
3DH	$V6 + (V5 - V6) \times 4 / 21.2$	$V10 + (V9 - V10) \times 17.2 / 21.2$
3EH	V6	V9
3FH	V7	V8

Absolute Maximum Ratings

	MIN.	MAX.	UNIT
Logic supply voltage, VCC Digital input voltage Output voltage, DIO1 & DIO2	-0.5	5	V
Analog supply voltage, AVDD Gamma voltage , V1~V14 OUT1 ~ OUT1200	-0.5	15	V

TEMPREATURE

	MIN.	MAX.	UNIT
Operating temperature	-30	85	°C
Storage temperature	-55	125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

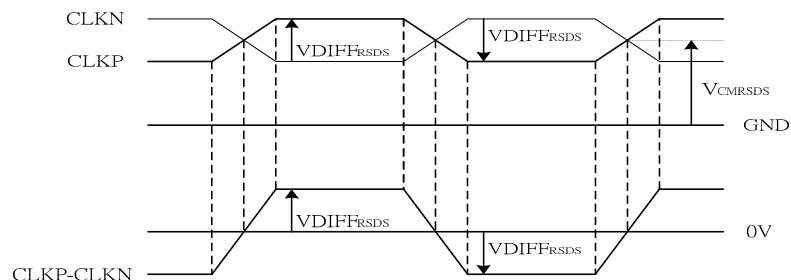
DC Electrical Characteristics

(For the digital circuit: Test Condition VCC =3.3V , AVDD= 10V, AVSS=GND=0V, TA=25°C)
TTL mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.7	3.3	3.6	V	Digital power : default 3.3V
Low Level Input Voltage	Vil	0	-	0.3xVCC	V	For the digital circuit
High Level Input Voltage	Vih	0.7xVCC	-	VCC	V	For the digital circuit
High Level Output Voltage	Voh	VCC-0.4	-	-	V	DIO1, DIO2, loh=1mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	DIO1, DIO2, lol=-1mA
Input Leakage Current	Ii	-	-	±1	uA	For the digital circuit
Digital Stand-by Current	Ist	-	10	50	uA	DCLK is stopped, Inputs are default, Outputs are High-Z.
Digital Operating Current	Icc	-	3	4	mA	Fclk=50 MHz, FLD=50KHz, VCC=3.3V
Pull low/ high resistor	Ri	150K	300K	-	ohm	Digital signal

RSDS mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.7	3.3	3.6	V	Digital power : default 3.3V
RSDS Low Level Input Voltage	Vilrsds	-	-200	-100	mV	D2[2:0]P,D2[2:0]N,CLKP,CLKN
RSDS High Level Input Voltage	Vihrsds	100	200	-	mV	D2[2:0]P,D2[2:0]N,CLKP,CLKN
RSDS reference Voltage	Vcmrsds	GND+0.1	1.2	VCC-1.2	V	D2[2:0]P,D2[2:0]N,CLKP,CLKN
Low Level Input Voltage	Vil	0	-	0.3xVCC	V	Other input pins
High Level Input Voltage	Vih	0.7xVCC	-	VCC	V	Other input pins
High Level Output Voltage	Voh	VCC-0.4	-	-	V	DIO1,DIO2,loh=1mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	DIO1,DIO2,lol=-1mA
RSDS input Leakage Current	Iirrsds	-	-	10	uA	D2[2:0]P,D2[2:0]N,CLKP,CLKN
Input Leakage Current	Ii	-	-	±1	uA	Other input pins
RSDS Digital Stand-by Current	Istrsds	-	-	600	uA	DCLK is stopped, Inputs are default, Outputs are High-Z.
RSDS Digital Operating Current	Iccrsds	-	-	7.5	mA	Fclk=50 MHz, FLD=50KHz, VCC=3.3V
Pull low/ high resistor	Ri	150K	300K	-	ohm	Digital signal



- NOTES: 1. $V_{CMRSDS} = (V_{CLKP} + V_{CLKN}) / 2$ OR $V_{CMRSDS} = (V_{DxxP} + V_{DxxN}) / 2$
2. $V_{DIFFRSDS} = V_{CLKP} - V_{CLKN}$ or $V_{DIFFRSDS} = V_{DxxP} - V_{DxxN}$

(For the analog circuit: Test Condition VCC =3.3V , AVDD= 10V, AVSS=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVDD	6.5	10	13.5	V	For the analog circuit power
Input level of V1 ~ V7	Vref	0.4AVDD	-	AVDD-0.1	V	Gamma correction voltage
Input level of V8 ~ V14	Vref	0.1	-	0.6AVDD	V	Gamma correction voltage
Output Voltage deviation	Vod	-	±20	-	mV	
Voltage Output Offset between Chips	Voc	-	±20	-	mV	
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	OUT1 ~ OUT1200
Sinking Current of Outputs	IOLy	80	-	-	uA	OUT1 ~ OUT1200; Vo=0.1V v.s 1.0V , AVDD=13.5V
	IOLr	400				RPO1,RPO2; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	OUT1 ~ OUT1200; Vo=13.4V v.s 12.5V , AVDD=13.5V
	IOHr	400				RPO1,RPO2; Vo=13.4V v.s 12.5V , AVDD=13.5V
Impedance of Gamma Correction	Rg	0.8*Rn	1.1*Rn	1.4*Rn	ohm	Rn: Internal gamma resistor
Analog Stand-by Current	Isc	-	8.5	10	mA	No load, AVDD=10V, and all operating is stopped
Analog Operating Current	Ioc	-	10	12	mA	No load, Fclk=50MHz, FLD=50KHz, AVDD=10V, V1=8V, V14=0.4V

AC Electrical Characteristics

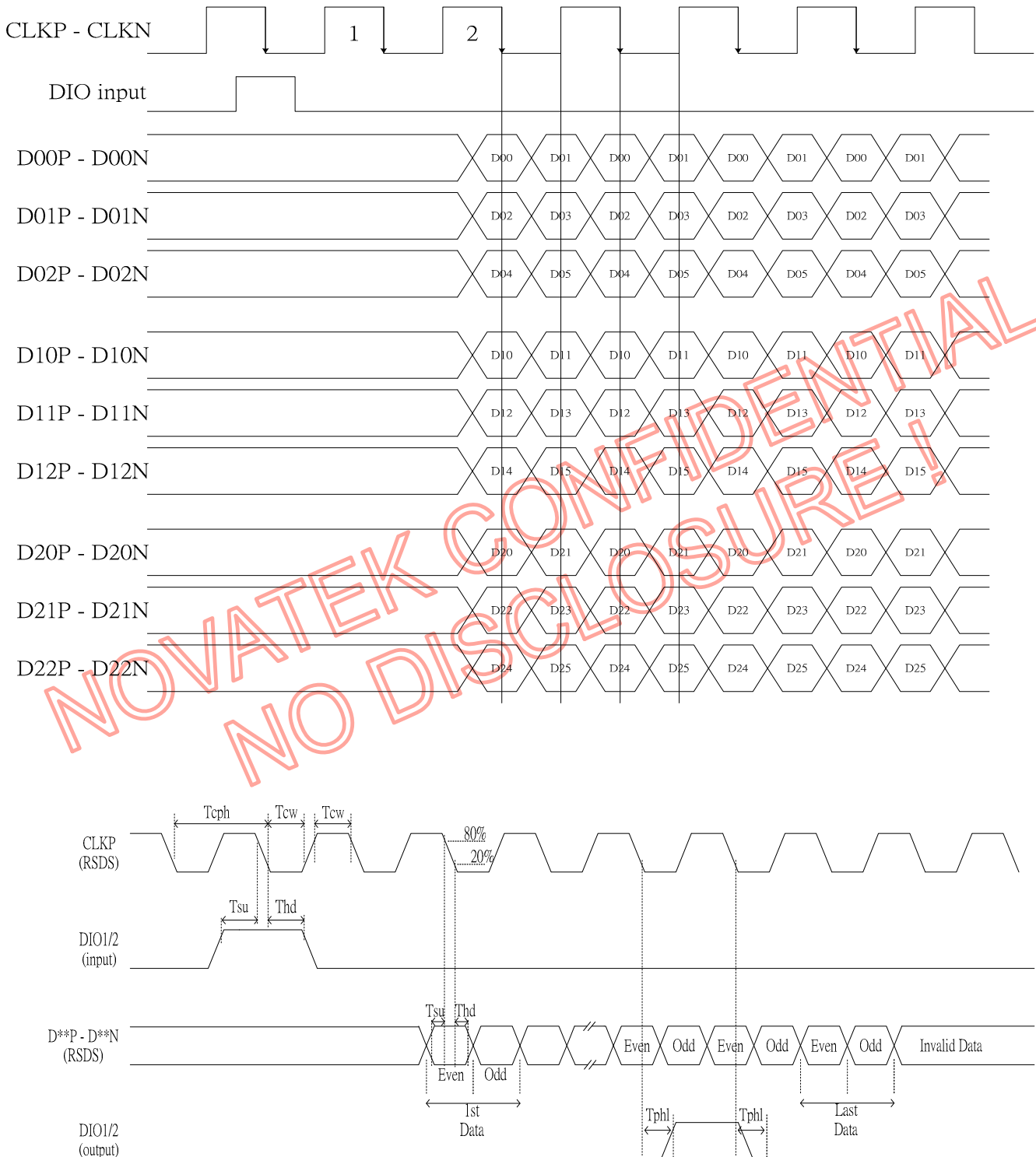
(VCC =3.3V, AVDD=10V, AVSS=GND=0V, TA= 25°C)

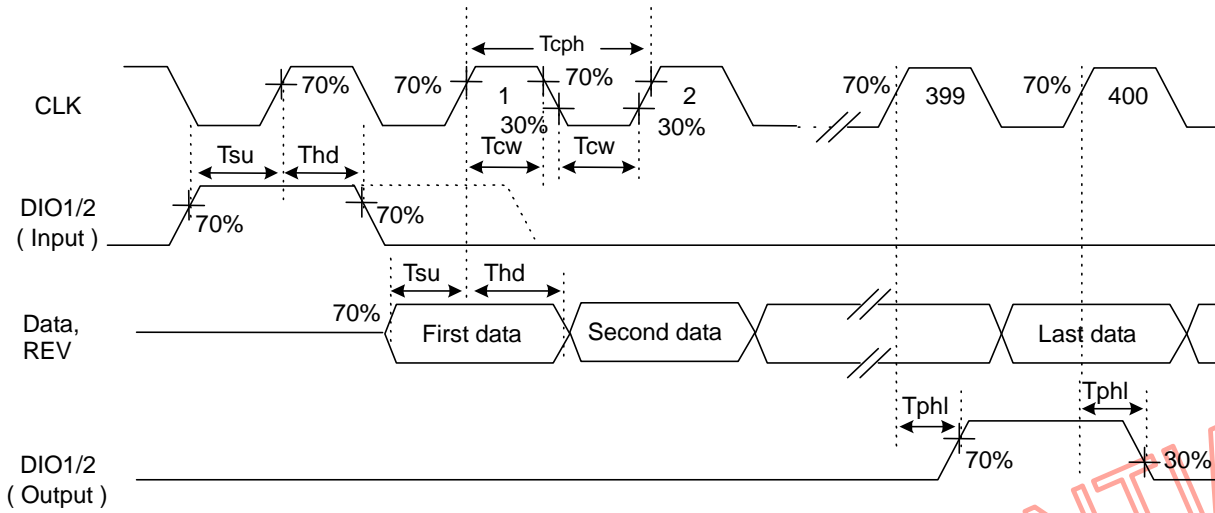
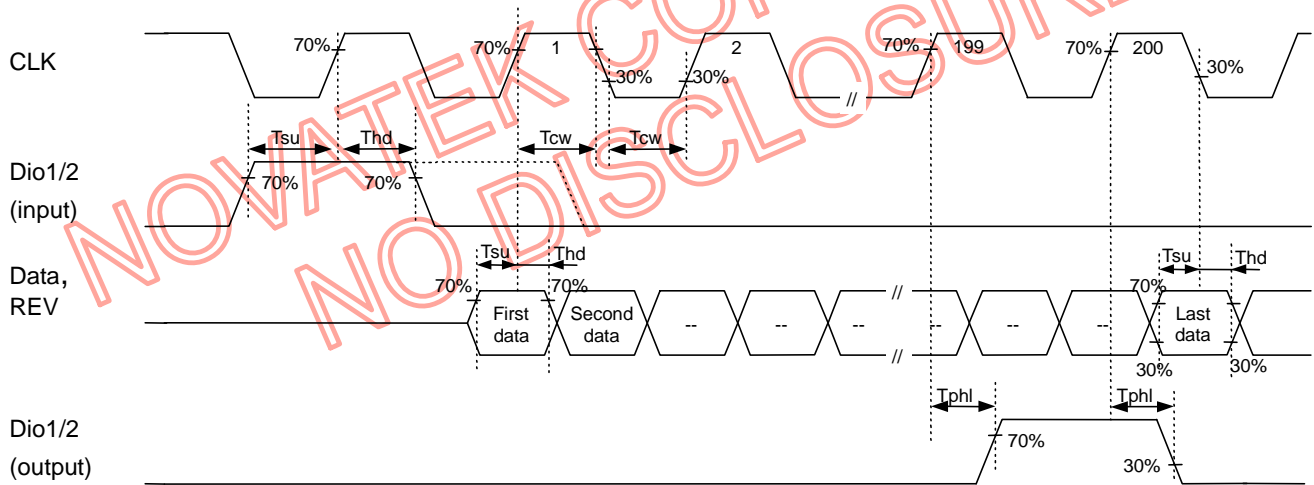
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	50	55	MHz	EDGSL = '0'
	Fclk	-	25	27.5	MHz	EDGSL = '1'
CLK pulse width	Tcw	40%	-	60%	Tcph	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	9	us	10% or 90% target voltage. CL=60pF, R=2K ohm
Repair output delay stable time	Tst1	-	-	20	us	CL=190pF, R=5.5K ohm

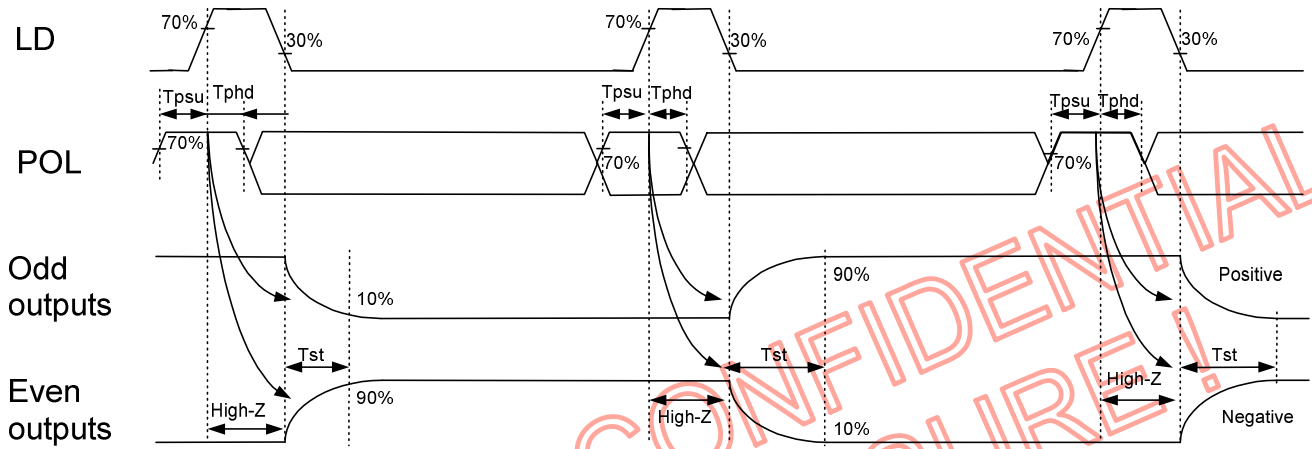
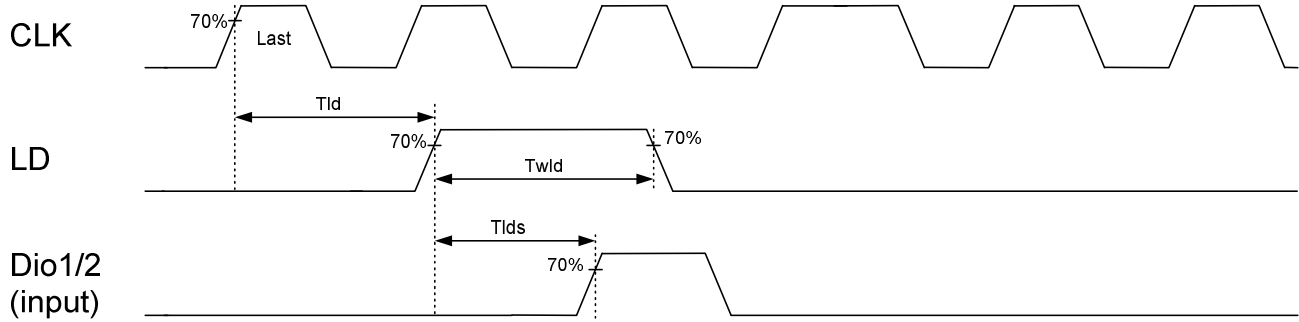
Timing Diagram

1. Clock and data input timing diagram 1

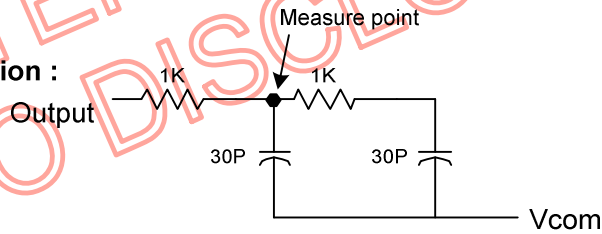
1.1 RSDS mode



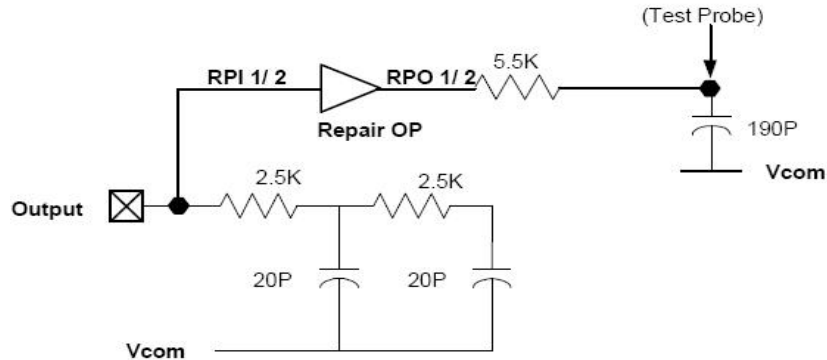
1.2 TTL mode
<< EDGSL= "0", Default >>

<< EDGSL= "1">>


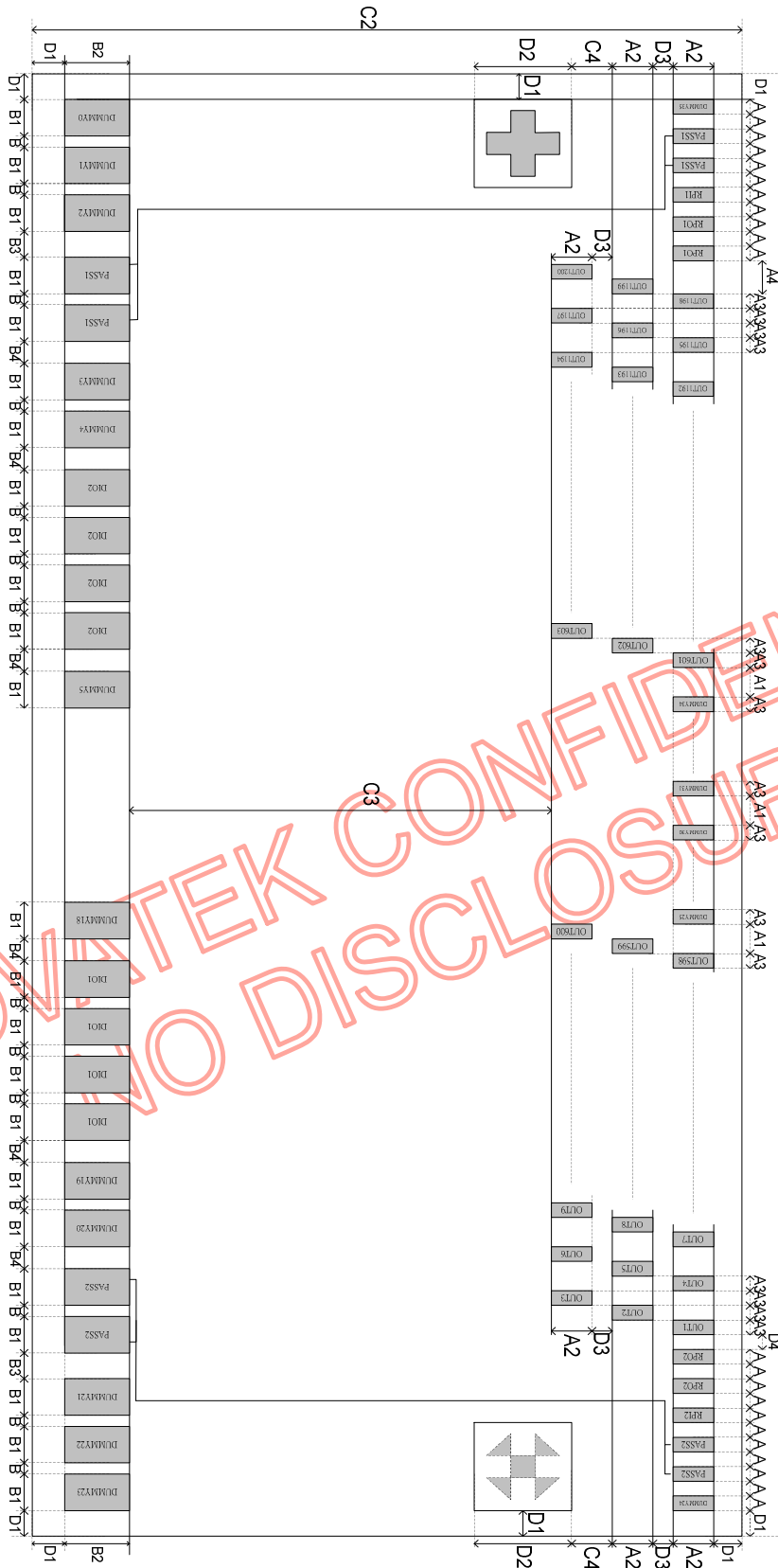
2. Clock and data input timing diagram 2


Output load condition :



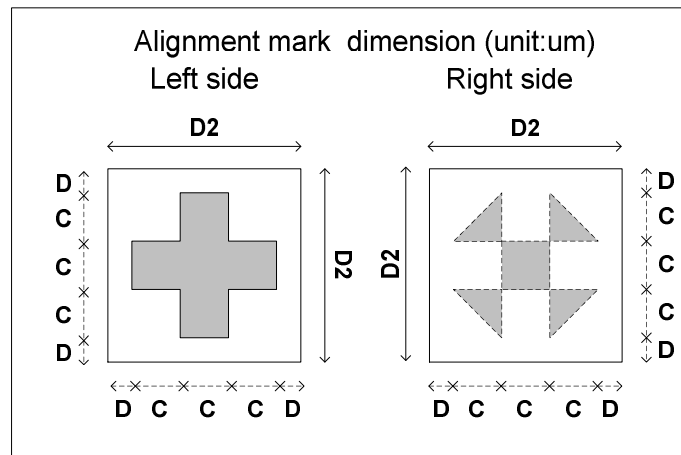
Repair OP output load condition :



Pad Outline Dimension (Bump Side)


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1. Alignment Mark

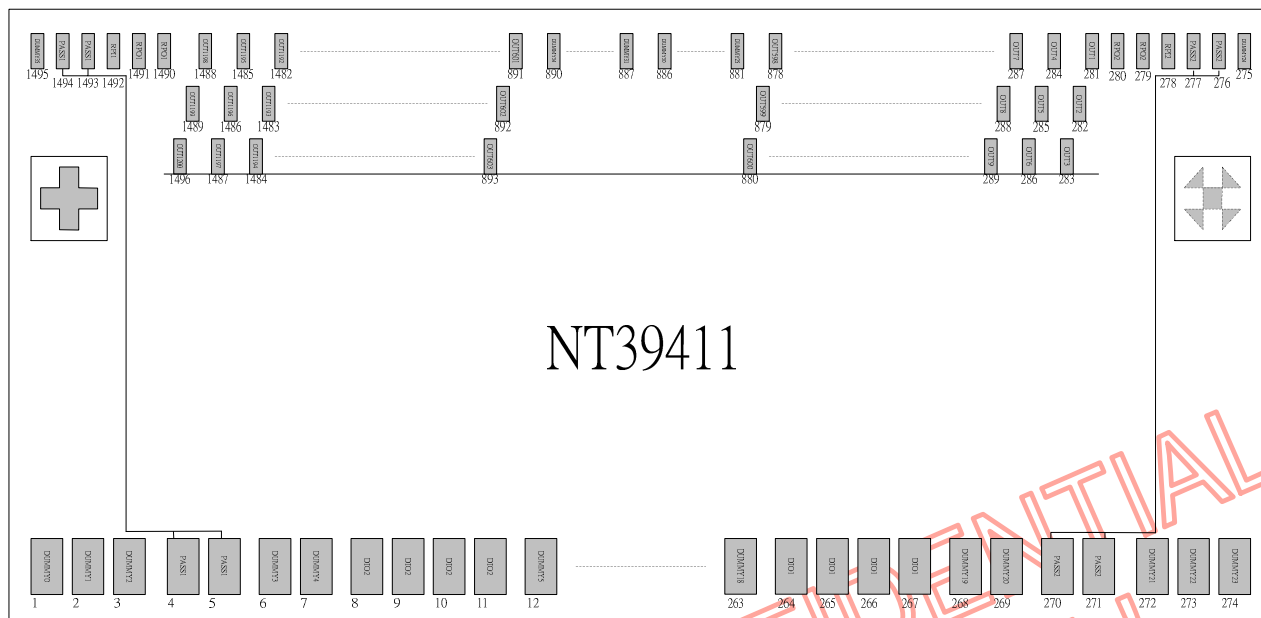


2. Pad Information

Symbol	Dimension in um	Symbol	Dimension in um
A	22	C	30
A1	38	C1	24056
A2	100	C2	1100
A3	19	C3	490
A4	59	C4	80
B	16	D	15
B1	66	D1	80
B2	90	D2	120
B3	38	D3	30
B4	36	D4	21

Chip size: 24056(X) x 1100(Y) um² (scribe line included)

Appendix A: Pad Coordinate



Pad	TextName	CX	CY
1	DUMMY[0]	-11915	-425
2	DUMMY[1]	-11833	-425
3	DUMMY[2]	-11751	-425
4	PASS1	-11647	-425
5	PASS1	-11565	-425
6	DUMMY[3]	-11463	-425
7	DUMMY[4]	-11381	-425
8	DIO2	-11279	-425
9	DIO2	-11197	-425
10	DIO2	-11115	-425
11	DIO2	-11033	-425
12	DUMMY[5]	-10931	-425
13	AVDD	-10829	-425
14	AVDD	-10747	-425
15	AVDD	-10665	-425
16	AVDD	-10583	-425
17	AVDD	-10501	-425
18	AVDD	-10419	-425
19	AVDD	-10337	-425
20	AVDD	-10255	-425
21	AVDD	-10173	-425
22	AVDD	-10091	-425
23	ENREOP	-9989	-425
24	ENREOP	-9907	-425
25	ENREOP	-9825	-425

26	CHNSL	-9723	-425
27	CHNSL	-9641	-425
28	CHNSL	-9559	-425
29	GND	-9457	-425
30	GND	-9375	-425
31	GND	-9293	-425
32	GND	-9211	-425
33	GND	-9129	-425
34	GND	-9047	-425
35	GND	-8965	-425
36	GND	-8883	-425
37	CHNSD	-8781	-425
38	CHNSD	-8699	-425
39	CHNSD	-8617	-425
40	VCC	-8515	-425
41	VCC	-8433	-425
42	VCC	-8351	-425
43	VCC	-8269	-425
44	VCC	-8187	-425
45	VCC	-8105	-425
46	VCC	-8023	-425
47	VCC	-7941	-425
48	DUMMY[6]	-7839	-425
49	POL	-7737	-425
50	POL	-7655	-425
51	POL	-7573	-425

52	POL	-7491	-425
53	DUMMY[7]	-7389	-425
54	REV	-7287	-425
55	REV	-7205	-425
56	REV	-7123	-425
57	REV	-7041	-425
58	DUMMY[8]	-6939	-425
59	LD	-6837	-425
60	LD	-6755	-425
61	LD	-6673	-425
62	LD	-6591	-425
63	DUMMY[9]	-6489	-425
64	D25	-6387	-425
65	D25	-6305	-425
66	D25	-6223	-425
67	D25	-6141	-425
68	D24	-6039	-425
69	D24	-5957	-425
70	D24	-5875	-425
71	D24	-5793	-425
72	D23	-5691	-425
73	D23	-5609	-425
74	D23	-5527	-425
75	D23	-5445	-425
76	D22	-5343	-425
77	D22	-5261	-425

78	D22	-5179	-425
79	D22	-5097	-425
80	D21	-4995	-425
81	D21	-4913	-425
82	D21	-4831	-425
83	D21	-4749	-425
84	D20	-4647	-425
85	D20	-4565	-425
86	D20	-4483	-425
87	D20	-4401	-425
88	DUMMY[10]	-4299	-425
89	AVSS	-4197	-425
90	AVSS	-4115	-425
91	AVSS	-4033	-425
92	AVSS	-3951	-425
93	AVSS	-3869	-425
94	AVSS	-3787	-425
95	AVSS	-3705	-425
96	AVSS	-3623	-425
97	AVSS	-3541	-425
98	AVSS	-3459	-425
99	DUMMY[11]	-3357	-425
100	V14	-3255	-425
101	V14	-3173	-425
102	V14	-3091	-425
103	V14	-3009	-425
104	V13	-2907	-425
105	V13	-2825	-425
106	V13	-2743	-425
107	V13	-2661	-425
108	V12	-2559	-425
109	V12	-2477	-425
110	V12	-2395	-425
111	V12	-2313	-425
112	V11	-2211	-425
113	V11	-2129	-425
114	V11	-2047	-425
115	V11	-1965	-425
116	V10	-1863	-425
117	V10	-1781	-425
118	V10	-1699	-425
119	V10	-1617	-425
120	V9	-1515	-425
121	V9	-1433	-425
122	V9	-1351	-425
123	V9	-1269	-425
124	V8	-1167	-425
125	V8	-1085	-425
126	V8	-1003	-425
127	V8	-921	-425
128	V7	-819	-425
129	V7	-737	-425
130	V7	-655	-425
131	V7	-573	-425
132	V6	-471	-425
133	V6	-389	-425
134	V6	-307	-425
135	V6	-225	-425
136	V5	-123	-425
137	V5	-41	-425
138	V5	41	-425
139	V5	123	-425
140	V4	225	-425
141	V4	307	-425
142	V4	389	-425
143	V4	471	-425

144	V3	573	-425
145	V3	655	-425
146	V3	737	-425
147	V3	819	-425
148	V2	921	-425
149	V2	1003	-425
150	V2	1085	-425
151	V2	1167	-425
152	V1	1269	-425
153	V1	1351	-425
154	V1	1433	-425
155	V1	1515	-425
156	DUMMY[12]	1617	-425
157	AVDD	1719	-425
158	AVDD	1801	-425
159	AVDD	1883	-425
160	AVDD	1965	-425
161	AVDD	2047	-425
162	AVDD	2129	-425
163	AVDD	2211	-425
164	AVDD	2293	-425
165	AVDD	2375	-425
166	AVDD	2457	-425
167	DUMMY[13]	2559	-425
168	D15	2661	-425
169	D15	2743	-425
170	D15	2825	-425
171	D15	2907	-425
172	D14	3009	-425
173	D14	3091	-425
174	D14	3173	-425
175	D14	3255	-425
176	D13	3357	-425
177	D13	3439	-425
178	D13	3521	-425
179	D13	3603	-425
180	D12	3705	-425
181	D12	3787	-425
182	D12	3869	-425
183	D12	3951	-425
184	D11	4053	-425
185	D11	4135	-425
186	D11	4217	-425
187	D11	4299	-425
188	D10	4401	-425
189	D10	4483	-425
190	D10	4565	-425
191	D10	4647	-425
192	D05	4749	-425
193	D05	4831	-425
194	D05	4913	-425
195	D05	4995	-425
196	D04	5097	-425
197	D04	5179	-425
198	D04	5261	-425
199	D04	5343	-425
200	D03	5445	-425
201	D03	5527	-425
202	D03	5609	-425
203	D03	5691	-425
204	D02	5793	-425
205	D02	5875	-425
206	D02	5957	-425
207	D02	6039	-425
208	D01	6141	-425
209	D01	6223	-425

210	D01	6305	-425
211	D01	6387	-425
212	D00	6489	-425
213	D00	6571	-425
214	D00	6653	-425
215	D00	6735	-425
216	DUMMY[14]	6837	-425
217	CLKN	6939	-425
218	CLKN	7021	-425
219	CLKN	7103	-425
220	CLKN	7185	-425
221	CLK	7287	-425
222	CLK	7369	-425
223	CLK	7451	-425
224	CLK	7533	-425
225	SHL	7635	-425
226	SHL	7717	-425
227	SHL	7799	-425
228	EDGSL	7901	-425
229	EDGSL	7983	-425
230	EDGSL	8065	-425
231	ITLRSDS	8167	-425
232	ITLRSDS	8249	-425
233	ITLRSDS	8331	-425
234	DUMMY[15]	8433	-425
235	VCC	8535	-425
236	VCC	8617	-425
237	VCC	8699	-425
238	VCC	8781	-425
239	VCC	8863	-425
240	VCC	8945	-425
241	VCC	9027	-425
242	VCC	9109	-425
243	DUMMY[16]	9211	-425
244	GND	9313	-425
245	GND	9395	-425
246	GND	9477	-425
247	GND	9559	-425
248	GND	9641	-425
249	GND	9723	-425
250	GND	9805	-425
251	GND	9887	-425
252	DUMMY[17]	9989	-425
253	AVSS	10091	-425
254	AVSS	10173	-425
255	AVSS	10255	-425
256	AVSS	10337	-425
257	AVSS	10419	-425
258	AVSS	10501	-425
259	AVSS	10583	-425
260	AVSS	10665	-425
261	AVSS	10747	-425
262	AVSS	10829	-425
263	DUMMY[18]	10931	-425
264	DIO1	11033	-425
265	DIO1	11115	-425
266	DIO1	11197	-425
267	DIO1	11279	-425
268	DUMMY[19]	11381	-425
269	DUMMY[20]	11463	-425
270	PASS2	11565	-425
271	PASS2	11647	-425
272	DUMMY[21]	11751	-425
273	DUMMY[22]	11833	-425
274	DUMMY[23]	11915	-425
275	DUMMY[24]	11937	420

276	PASS2	11893	420
277	PASS2	11849	420
278	RPI2	11805	420
279	RPO2	11761	420
280	RPO2	11717	420
281	OUT[1]	11675.5	420
282	OUT[2]	11656.5	290
283	OUT[3]	11637.5	160
284	OUT[4]	11618.5	420
285	OUT[5]	11599.5	290
286	OUT[6]	11580.5	160
287	OUT[7]	11561.5	420
288	OUT[8]	11542.5	290
289	OUT[9]	11523.5	160
290	OUT[10]	11504.5	420
291	OUT[11]	11485.5	290
292	OUT[12]	11466.5	160
293	OUT[13]	11447.5	420
294	OUT[14]	11428.5	290
295	OUT[15]	11409.5	160
296	OUT[16]	11390.5	420
297	OUT[17]	11371.5	290
298	OUT[18]	11352.5	160
299	OUT[19]	11333.5	420
300	OUT[20]	11314.5	290
301	OUT[21]	11295.5	160
302	OUT[22]	11276.5	420
303	OUT[23]	11257.5	290
304	OUT[24]	11238.5	160
305	OUT[25]	11219.5	420
306	OUT[26]	11200.5	290
307	OUT[27]	11181.5	160
308	OUT[28]	11162.5	420
309	OUT[29]	11143.5	290
310	OUT[30]	11124.5	160
311	OUT[31]	11105.5	420
312	OUT[32]	11086.5	290
313	OUT[33]	11067.5	160
314	OUT[34]	11048.5	420
315	OUT[35]	11029.5	290
316	OUT[36]	11010.5	160
317	OUT[37]	10991.5	420
318	OUT[38]	10972.5	290
319	OUT[39]	10953.5	160
320	OUT[40]	10934.5	420
321	OUT[41]	10915.5	290
322	OUT[42]	10896.5	160
323	OUT[43]	10877.5	420
324	OUT[44]	10858.5	290
325	OUT[45]	10839.5	160
326	OUT[46]	10820.5	420
327	OUT[47]	10801.5	290
328	OUT[48]	10782.5	160
329	OUT[49]	10763.5	420
330	OUT[50]	10744.5	290
331	OUT[51]	10725.5	160
332	OUT[52]	10706.5	420
333	OUT[53]	10687.5	290
334	OUT[54]	10668.5	160
335	OUT[55]	10649.5	420
336	OUT[56]	10630.5	290
337	OUT[57]	10611.5	160
338	OUT[58]	10592.5	420
339	OUT[59]	10573.5	290
340	OUT[60]	10554.5	160
341	OUT[61]	10535.5	420

342	OUT[62]	10516.5	290
343	OUT[63]	10497.5	160
344	OUT[64]	10478.5	420
345	OUT[65]	10459.5	290
346	OUT[66]	10440.5	160
347	OUT[67]	10421.5	420
348	OUT[68]	10402.5	290
349	OUT[69]	10383.5	160
350	OUT[70]	10364.5	420
351	OUT[71]	10345.5	290
352	OUT[72]	10326.5	160
353	OUT[73]	10307.5	420
354	OUT[74]	10288.5	290
355	OUT[75]	10269.5	160
356	OUT[76]	10250.5	420
357	OUT[77]	10231.5	290
358	OUT[78]	10212.5	160
359	OUT[79]	10193.5	420
360	OUT[80]	10174.5	290
361	OUT[81]	10155.5	160
362	OUT[82]	10136.5	420
363	OUT[83]	10117.5	290
364	OUT[84]	10098.5	160
365	OUT[85]	10079.5	420
366	OUT[86]	10060.5	290
367	OUT[87]	10041.5	160
368	OUT[88]	10022.5	420
369	OUT[89]	10003.5	290
370	OUT[90]	9984.5	160
371	OUT[91]	9965.5	420
372	OUT[92]	9946.5	290
373	OUT[93]	9927.5	160
374	OUT[94]	9908.5	420
375	OUT[95]	9889.5	290
376	OUT[96]	9870.5	160
377	OUT[97]	9851.5	420
378	OUT[98]	9832.5	290
379	OUT[99]	9813.5	160
380	OUT[100]	9794.5	420
381	OUT[101]	9775.5	290
382	OUT[102]	9756.5	160
383	OUT[103]	9737.5	420
384	OUT[104]	9718.5	290
385	OUT[105]	9699.5	160
386	OUT[106]	9680.5	420
387	OUT[107]	9661.5	290
388	OUT[108]	9642.5	160
389	OUT[109]	9623.5	420
390	OUT[110]	9604.5	290
391	OUT[111]	9585.5	160
392	OUT[112]	9566.5	420
393	OUT[113]	9547.5	290
394	OUT[114]	9528.5	160
395	OUT[115]	9509.5	420
396	OUT[116]	9490.5	290
397	OUT[117]	9471.5	160
398	OUT[118]	9452.5	420
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400	OUT[120]	9414.5	160
401	OUT[121]	9395.5	420
402	OUT[122]	9376.5	290
403	OUT[123]	9357.5	160
404	OUT[124]	9338.5	420
405	OUT[125]	9319.5	290
406	OUT[126]	9300.5	160
407	OUT[127]	9281.5	420

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409	OUT[129]	9243.5	160
410	OUT[130]	9224.5	420
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412	OUT[132]	9186.5	160
413	OUT[133]	9167.5	420
414	OUT[134]	9148.5	290
415	OUT[135]	9129.5	160
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417	OUT[137]	9091.5	290
418	OUT[138]	9072.5	160
419	OUT[139]	9053.5	420
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421	OUT[141]	9015.5	160
422	OUT[142]	8996.5	420
423	OUT[143]	8977.5	290
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427	OUT[147]	8901.5	160
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433	OUT[153]	8787.5	160
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442	OUT[162]	8616.5	160
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445	OUT[165]	8559.5	160
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453	OUT[173]	8407.5	290
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457	OUT[177]	8331.5	160
458	OUT[178]	8312.5	420
459	OUT[179]	8293.5	290
460	OUT[180]	8274.5	160
461	OUT[181]	8255.5	420
462	OUT[182]	8236.5	290
463	OUT[183]	8217.5	160
464	OUT[184]	8198.5	420
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468	OUT[188]	8122.5	290
469	OUT[189]	8103.5	160
470	OUT[190]	8084.5	420
471	OUT[191]	8065.5	290
472	OUT[192]	8046.5	160
473	OUT[193]	8027.5	420

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493	OUT[213]	7647.5	160
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622	OUT[342]	5196.5	160
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625	OUT[345]	5139.5	160
626	OUT[346]	5120.5	420
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637	OUT[357]	4911.5	160
638	OUT[358]	4892.5	420
639	OUT[359]	4873.5	290
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646	OUT[366]	4740.5	160
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667	OUT[387]	4341.5	160
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669	OUT[389]	4303.5	290
670	OUT[390]	4284.5	160
671	OUT[391]	4265.5	420

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674	OUT[394]	4208.5	420
675	OUT[395]	4189.5	290
676	OUT[396]	4170.5	160
677	OUT[397]	4151.5	420
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683	OUT[403]	4037.5	420
684	OUT[404]	4018.5	290
685	OUT[405]	3999.5	160
686	OUT[406]	3980.5	420
687	OUT[407]	3961.5	290
688	OUT[408]	3942.5	160
689	OUT[409]	3923.5	420
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692	OUT[412]	3866.5	420
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697	OUT[417]	3771.5	160
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701	OUT[421]	3695.5	420
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703	OUT[423]	3657.5	160
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706	OUT[426]	3600.5	160
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709	OUT[429]	3543.5	160
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713	OUT[433]	3467.5	420
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715	OUT[435]	3429.5	160
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717	OUT[437]	3391.5	290
718	OUT[438]	3372.5	160
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721	OUT[441]	3315.5	160
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723	OUT[443]	3277.5	290
724	OUT[444]	3258.5	160
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727	OUT[447]	3201.5	160
728	OUT[448]	3182.5	420
729	OUT[449]	3163.5	290
730	OUT[450]	3144.5	160
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734	OUT[454]	3068.5	420
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736	OUT[456]	3030.5	160
737	OUT[457]	3011.5	420

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739	OUT[459]	2973.5	160
740	OUT[460]	2954.5	420
741	OUT[461]	2935.5	290
742	OUT[462]	2916.5	160
743	OUT[463]	2897.5	420
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745	OUT[465]	2859.5	160
746	OUT[466]	2840.5	420
747	OUT[467]	2821.5	290
748	OUT[468]	2802.5	160
749	OUT[469]	2783.5	420
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753	OUT[473]	2707.5	290
754	OUT[474]	2688.5	160
755	OUT[475]	2669.5	420
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773	OUT[493]	2327.5	420
774	OUT[494]	2308.5	290
775	OUT[495]	2289.5	160
776	OUT[496]	2270.5	420
777	OUT[497]	2251.5	290
778	OUT[498]	2232.5	160
779	OUT[499]	2213.5	420
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781	OUT[501]	2175.5	160
782	OUT[502]	2156.5	420
783	OUT[503]	2137.5	290
784	OUT[504]	2118.5	160
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786	OUT[506]	2080.5	290
787	OUT[507]	2061.5	160
788	OUT[508]	2042.5	420
789	OUT[509]	2023.5	290
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791	OUT[511]	1985.5	420
792	OUT[512]	1966.5	290
793	OUT[513]	1947.5	160
794	OUT[514]	1928.5	420
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796	OUT[516]	1890.5	160
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801	OUT[521]	1795.5	290
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803	OUT[523]	1757.5	420

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809	OUT[529]	1643.5	420
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812	OUT[532]	1586.5	420
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814	OUT[534]	1548.5	160
815	OUT[535]	1529.5	420
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817	OUT[537]	1491.5	160
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820	OUT[540]	1434.5	160
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822	OUT[542]	1396.5	290
823	OUT[543]	1377.5	160
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842	OUT[562]	1016.5	420
843	OUT[563]	997.5	290
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849	OUT[569]	883.5	290
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855	OUT[575]	769.5	290
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858	OUT[578]	712.5	290
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860	OUT[580]	674.5	420
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866	OUT[586]	560.5	420
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869	OUT[589]	503.5	420

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872	OUT[592]	446.5	420
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874	OUT[594]	408.5	160
875	OUT[595]	389.5	420
876	OUT[596]	370.5	290
877	OUT[597]	351.5	160
878	OUT[598]	332.5	420
879	OUT[599]	313.5	290
880	OUT[600]	294.5	160
881	DUMMY[25]	275.5	420
882	DUMMY[26]	218.5	420
883	DUMMY[27]	161.5	420
884	DUMMY[28]	104.5	420
885	DUMMY[29]	47.5	420
886	DUMMY[30]	-9.5	420
887	DUMMY[31]	-66.5	420
888	DUMMY[32]	-123.5	420
889	DUMMY[33]	-180.5	420
890	DUMMY[34]	-237.5	420
891	OUT[601]	-294.5	420
892	OUT[602]	-313.5	290
893	OUT[603]	-332.5	160
894	OUT[604]	-351.5	420
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896	OUT[606]	-389.5	160
897	OUT[607]	-408.5	420
898	OUT[608]	-427.5	290
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900	OUT[610]	-465.5	420
901	OUT[611]	-484.5	290
902	OUT[612]	-503.5	160
903	OUT[613]	-522.5	420
904	OUT[614]	-541.5	290
905	OUT[615]	-560.5	160
906	OUT[616]	-579.5	420
907	OUT[617]	-598.5	290
908	OUT[618]	-617.5	160
909	OUT[619]	-636.5	420
910	OUT[620]	-655.5	290
911	OUT[621]	-674.5	160
912	OUT[622]	-693.5	420
913	OUT[623]	-712.5	290
914	OUT[624]	-731.5	160
915	OUT[625]	-750.5	420
916	OUT[626]	-769.5	290
917	OUT[627]	-788.5	160
918	OUT[628]	-807.5	420
919	OUT[629]	-826.5	290
920	OUT[630]	-845.5	160
921	OUT[631]	-864.5	420
922	OUT[632]	-883.5	290
923	OUT[633]	-902.5	160
924	OUT[634]	-921.5	420
925	OUT[635]	-940.5	290
926	OUT[636]	-959.5	160
927	OUT[637]	-978.5	420
928	OUT[638]	-997.5	290
929	OUT[639]	-1016.5	160
930	OUT[640]	-1035.5	420
931	OUT[641]	-1054.5	290
932	OUT[642]	-1073.5	160
933	OUT[643]	-1092.5	420
934	OUT[644]	-1111.5	290
935	OUT[645]	-1130.5	160

936	OUT[646]	-1149.5	420
937	OUT[647]	-1168.5	290
938	OUT[648]	-1187.5	160
939	OUT[649]	-1206.5	420
940	OUT[650]	-1225.5	290
941	OUT[651]	-1244.5	160
942	OUT[652]	-1263.5	420
943	OUT[653]	-1282.5	290
944	OUT[654]	-1301.5	160
945	OUT[655]	-1320.5	420
946	OUT[656]	-1339.5	290
947	OUT[657]	-1358.5	160
948	OUT[658]	-1377.5	420
949	OUT[659]	-1396.5	290
950	OUT[660]	-1415.5	160
951	OUT[661]	-1434.5	420
952	OUT[662]	-1453.5	290
953	OUT[663]	-1472.5	160
954	OUT[664]	-1491.5	420
955	OUT[665]	-1510.5	290
956	OUT[666]	-1529.5	160
957	OUT[667]	-1548.5	420
958	OUT[668]	-1567.5	290
959	OUT[669]	-1586.5	160
960	OUT[670]	-1605.5	420
961	OUT[671]	-1624.5	290
962	OUT[672]	-1643.5	160
963	OUT[673]	-1662.5	420
964	OUT[674]	-1681.5	290
965	OUT[675]	-1700.5	160
966	OUT[676]	-1719.5	420
967	OUT[677]	-1738.5	290
968	OUT[678]	-1757.5	160
969	OUT[679]	-1776.5	420
970	OUT[680]	-1795.5	290
971	OUT[681]	-1814.5	160
972	OUT[682]	-1833.5	420
973	OUT[683]	-1852.5	290
974	OUT[684]	-1871.5	160
975	OUT[685]	-1890.5	420
976	OUT[686]	-1909.5	290
977	OUT[687]	-1928.5	160
978	OUT[688]	-1947.5	420
979	OUT[689]	-1966.5	290
980	OUT[690]	-1985.5	160
981	OUT[691]	-2004.5	420
982	OUT[692]	-2023.5	290
983	OUT[693]	-2042.5	160
984	OUT[694]	-2061.5	420
985	OUT[695]	-2080.5	290
986	OUT[696]	-2099.5	160
987	OUT[697]	-2118.5	420
988	OUT[698]	-2137.5	290
989	OUT[699]	-2156.5	160
990	OUT[700]	-2175.5	420
991	OUT[701]	-2194.5	290
992	OUT[702]	-2213.5	160
993	OUT[703]	-2232.5	420
994	OUT[704]	-2251.5	290
995	OUT[705]	-2270.5	160
996	OUT[706]	-2289.5	420
997	OUT[707]	-2308.5	290
998	OUT[708]	-2327.5	160
999	OUT[709]	-2346.5	420
1000	OUT[710]	-2365.5	290
1001	OUT[711]	-2384.5	160

1002	OUT[712]	-2403.5	420
1003	OUT[713]	-2422.5	290
1004	OUT[714]	-2441.5	160
1005	OUT[715]	-2460.5	420
1006	OUT[716]	-2479.5	290
1007	OUT[717]	-2498.5	160
1008	OUT[718]	-2517.5	420
1009	OUT[719]	-2536.5	290
1010	OUT[720]	-2555.5	160
1011	OUT[721]	-2574.5	420
1012	OUT[722]	-2593.5	290
1013	OUT[723]	-2612.5	160
1014	OUT[724]	-2631.5	420
1015	OUT[725]	-2650.5	290
1016	OUT[726]	-2669.5	160
1017	OUT[727]	-2688.5	420
1018	OUT[728]	-2707.5	290
1019	OUT[729]	-2726.5	160
1020	OUT[730]	-2745.5	420
1021	OUT[731]	-2764.5	290
1022	OUT[732]	-2783.5	160
1023	OUT[733]	-2802.5	420
1024	OUT[734]	-2821.5	290
1025	OUT[735]	-2840.5	160
1026	OUT[736]	-2859.5	420
1027	OUT[737]	-2878.5	290
1028	OUT[738]	-2897.5	160
1029	OUT[739]	-2916.5	420
1030	OUT[740]	-2935.5	290
1031	OUT[741]	-2954.5	160
1032	OUT[742]	-2973.5	420
1033	OUT[743]	-2992.5	290
1034	OUT[744]	-3011.5	160
1035	OUT[745]	-3030.5	420
1036	OUT[746]	-3049.5	290
1037	OUT[747]	-3068.5	160
1038	OUT[748]	-3087.5	420
1039	OUT[749]	-3106.5	290
1040	OUT[750]	-3125.5	160
1041	OUT[751]	-3144.5	420
1042	OUT[752]	-3163.5	290
1043	OUT[753]	-3182.5	160
1044	OUT[754]	-3201.5	420
1045	OUT[755]	-3220.5	290
1046	OUT[756]	-3239.5	160
1047	OUT[757]	-3258.5	420
1048	OUT[758]	-3277.5	290
1049	OUT[759]	-3296.5	160
1050	OUT[760]	-3315.5	420
1051	OUT[761]	-3334.5	290
1052	OUT[762]	-3353.5	160
1053	OUT[763]	-3372.5	420
1054	OUT[764]	-3391.5	290
1055	OUT[765]	-3410.5	160
1056	OUT[766]	-3429.5	420
1057	OUT[767]	-3448.5	290
1058	OUT[768]	-3467.5	160
1059	OUT[769]	-3486.5	420
1060	OUT[770]	-3505.5	290
1061	OUT[771]	-3524.5	160
1062	OUT[772]	-3543.5	420
1063	OUT[773]	-3562.5	290
1064	OUT[774]	-3581.5	160
1065	OUT[775]	-3600.5	420
1066	OUT[776]	-3619.5	290
1067	OUT[777]	-3638.5	160

1068	OUT[778]	-3657.5	420
1069	OUT[779]	-3676.5	290
1070	OUT[780]	-3695.5	160
1071	OUT[781]	-3714.5	420
1072	OUT[782]	-3733.5	290
1073	OUT[783]	-3752.5	160
1074	OUT[784]	-3771.5	420
1075	OUT[785]	-3790.5	290
1076	OUT[786]	-3809.5	160
1077	OUT[787]	-3828.5	420
1078	OUT[788]	-3847.5	290
1079	OUT[789]	-3866.5	160
1080	OUT[790]	-3885.5	420
1081	OUT[791]	-3904.5	290
1082	OUT[792]	-3923.5	160
1083	OUT[793]	-3942.5	420
1084	OUT[794]	-3961.5	290
1085	OUT[795]	-3980.5	160
1086	OUT[796]	-3999.5	420
1087	OUT[797]	-4018.5	290
1088	OUT[798]	-4037.5	160
1089	OUT[799]	-4056.5	420
1090	OUT[800]	-4075.5	290
1091	OUT[801]	-4094.5	160
1092	OUT[802]	-4113.5	420
1093	OUT[803]	-4132.5	290
1094	OUT[804]	-4151.5	160
1095	OUT[805]	-4170.5	420
1096	OUT[806]	-4189.5	290
1097	OUT[807]	-4208.5	160
1098	OUT[808]	-4227.5	420
1099	OUT[809]	-4246.5	290
1100	OUT[810]	-4265.5	160
1101	OUT[811]	-4284.5	420
1102	OUT[812]	-4303.5	290
1103	OUT[813]	-4322.5	160
1104	OUT[814]	-4341.5	420
1105	OUT[815]	-4360.5	290
1106	OUT[816]	-4379.5	160
1107	OUT[817]	-4398.5	420
1108	OUT[818]	-4417.5	290
1109	OUT[819]	-4436.5	160
1110	OUT[820]	-4455.5	420
1111	OUT[821]	-4474.5	290
1112	OUT[822]	-4493.5	160
1113	OUT[823]	-4512.5	420
1114	OUT[824]	-4531.5	290
1115	OUT[825]	-4550.5	160
1116	OUT[826]	-4569.5	420
1117	OUT[827]	-4588.5	290
1118	OUT[828]	-4607.5	160
1119	OUT[829]	-4626.5	420
1120	OUT[830]	-4645.5	290
1121	OUT[831]	-4664.5	160
1122	OUT[832]	-4683.5	420
1123	OUT[833]	-4702.5	290
1124	OUT[834]	-4721.5	160
1125	OUT[835]	-4740.5	420
1126	OUT[836]	-4759.5	290
1127	OUT[837]	-4778.5	160
1128	OUT[838]	-4797.5	420
1129	OUT[839]	-4816.5	290
1130	OUT[840]	-4835.5	160
1131	OUT[841]	-4854.5	420
1132	OUT[842]	-4873.5	290
1133	OUT[843]	-4892.5	160

1134	OUT[844]	-4911.5	420
1135	OUT[845]	-4930.5	290
1136	OUT[846]	-4949.5	160
1137	OUT[847]	-4968.5	420
1138	OUT[848]	-4987.5	290
1139	OUT[849]	-5006.5	160
1140	OUT[850]	-5025.5	420
1141	OUT[851]	-5044.5	290
1142	OUT[852]	-5063.5	160
1143	OUT[853]	-5082.5	420
1144	OUT[854]	-5101.5	290
1145	OUT[855]	-5120.5	160
1146	OUT[856]	-5139.5	420
1147	OUT[857]	-5158.5	290
1148	OUT[858]	-5177.5	160
1149	OUT[859]	-5196.5	420
1150	OUT[860]	-5215.5	290
1151	OUT[861]	-5234.5	160
1152	OUT[862]	-5253.5	420
1153	OUT[863]	-5272.5	290
1154	OUT[864]	-5291.5	160
1155	OUT[865]	-5310.5	420
1156	OUT[866]	-5329.5	290
1157	OUT[867]	-5348.5	160
1158	OUT[868]	-5367.5	420
1159	OUT[869]	-5386.5	290
1160	OUT[870]	-5405.5	160
1161	OUT[871]	-5424.5	420
1162	OUT[872]	-5443.5	290
1163	OUT[873]	-5462.5	160
1164	OUT[874]	-5481.5	420
1165	OUT[875]	-5500.5	290
1166	OUT[876]	-5519.5	160
1167	OUT[877]	-5538.5	420
1168	OUT[878]	-5557.5	290
1169	OUT[879]	-5576.5	160
1170	OUT[880]	-5595.5	420
1171	OUT[881]	-5614.5	290
1172	OUT[882]	-5633.5	160
1173	OUT[883]	-5652.5	420
1174	OUT[884]	-5671.5	290
1175	OUT[885]	-5690.5	160
1176	OUT[886]	-5709.5	420
1177	OUT[887]	-5728.5	290
1178	OUT[888]	-5747.5	160
1179	OUT[889]	-5766.5	420
1180	OUT[890]	-5785.5	290
1181	OUT[891]	-5804.5	160
1182	OUT[892]	-5823.5	420
1183	OUT[893]	-5842.5	290
1184	OUT[894]	-5861.5	160
1185	OUT[895]	-5880.5	420
1186	OUT[896]	-5899.5	290
1187	OUT[897]	-5918.5	160
1188	OUT[898]	-5937.5	420
1189	OUT[899]	-5956.5	290
1190	OUT[900]	-5975.5	160
1191	OUT[901]	-5994.5	420
1192	OUT[902]	-6013.5	290
1193	OUT[903]	-6032.5	160
1194	OUT[904]	-6051.5	420
1195	OUT[905]	-6070.5	290
1196	OUT[906]	-6089.5	160
1197	OUT[907]	-6108.5	420
1198	OUT[908]	-6127.5	290
1199	OUT[909]	-6146.5	160

1200	OUT[910]	-6165.5	420
1201	OUT[911]	-6184.5	290
1202	OUT[912]	-6203.5	160
1203	OUT[913]	-6222.5	420
1204	OUT[914]	-6241.5	290
1205	OUT[915]	-6260.5	160
1206	OUT[916]	-6279.5	420
1207	OUT[917]	-6298.5	290
1208	OUT[918]	-6317.5	160
1209	OUT[919]	-6336.5	420
1210	OUT[920]	-6355.5	290
1211	OUT[921]	-6374.5	160
1212	OUT[922]	-6393.5	420
1213	OUT[923]	-6412.5	290
1214	OUT[924]	-6431.5	160
1215	OUT[925]	-6450.5	420
1216	OUT[926]	-6469.5	290
1217	OUT[927]	-6488.5	160
1218	OUT[928]	-6507.5	420
1219	OUT[929]	-6526.5	290
1220	OUT[930]	-6545.5	160
1221	OUT[931]	-6564.5	420
1222	OUT[932]	-6583.5	290
1223	OUT[933]	-6602.5	160
1224	OUT[934]	-6621.5	420
1225	OUT[935]	-6640.5	290
1226	OUT[936]	-6659.5	160
1227	OUT[937]	-6678.5	420
1228	OUT[938]	-6697.5	290
1229	OUT[939]	-6716.5	160
1230	OUT[940]	-6735.5	420
1231	OUT[941]	-6754.5	290
1232	OUT[942]	-6773.5	160
1233	OUT[943]	-6792.5	420
1234	OUT[944]	-6811.5	290
1235	OUT[945]	-6830.5	160
1236	OUT[946]	-6849.5	420
1237	OUT[947]	-6868.5	290
1238	OUT[948]	-6887.5	160
1239	OUT[949]	-6906.5	420
1240	OUT[950]	-6925.5	290
1241	OUT[951]	-6944.5	160
1242	OUT[952]	-6963.5	420
1243	OUT[953]	-6982.5	290
1244	OUT[954]	-7001.5	160
1245	OUT[955]	-7020.5	420
1246	OUT[956]	-7039.5	290
1247	OUT[957]	-7058.5	160
1248	OUT[958]	-7077.5	420
1249	OUT[959]	-7096.5	290
1250	OUT[960]	-7115.5	160
1251	OUT[961]	-7134.5	420
1252	OUT[962]	-7153.5	290
1253	OUT[963]	-7172.5	160
1254	OUT[964]	-7191.5	420
1255	OUT[965]	-7210.5	290
1256	OUT[966]	-7229.5	160
1257	OUT[967]	-7248.5	420
1258	OUT[968]	-7267.5	290
1259	OUT[969]	-7286.5	160
1260	OUT[970]	-7305.5	420
1261	OUT[971]	-7324.5	290
1262	OUT[972]	-7343.5	160
1263	OUT[973]	-7362.5	420
1264	OUT[974]	-7381.5	290
1265	OUT[975]	-7400.5	160

1266	OUT[976]	-7419.5	420
1267	OUT[977]	-7438.5	290
1268	OUT[978]	-7457.5	160
1269	OUT[979]	-7476.5	420
1270	OUT[980]	-7495.5	290
1271	OUT[981]	-7514.5	160
1272	OUT[982]	-7533.5	420
1273	OUT[983]	-7552.5	290
1274	OUT[984]	-7571.5	160
1275	OUT[985]	-7590.5	420
1276	OUT[986]	-7609.5	290
1277	OUT[987]	-7628.5	160
1278	OUT[988]	-7647.5	420
1279	OUT[989]	-7666.5	290
1280	OUT[990]	-7685.5	160
1281	OUT[991]	-7704.5	420
1282	OUT[992]	-7723.5	290
1283	OUT[993]	-7742.5	160
1284	OUT[994]	-7761.5	420
1285	OUT[995]	-7780.5	290
1286	OUT[996]	-7799.5	160
1287	OUT[997]	-7818.5	420
1288	OUT[998]	-7837.5	290
1289	OUT[999]	-7856.5	160
1290	OUT[1000]	-7875.5	420
1291	OUT[1001]	-7894.5	290
1292	OUT[1002]	-7913.5	160
1293	OUT[1003]	-7932.5	420
1294	OUT[1004]	-7951.5	290
1295	OUT[1005]	-7970.5	160
1296	OUT[1006]	-7989.5	420
1297	OUT[1007]	-8008.5	290
1298	OUT[1008]	-8027.5	160
1299	OUT[1009]	-8046.5	420
1300	OUT[1010]	-8065.5	290
1301	OUT[1011]	-8084.5	160
1302	OUT[1012]	-8103.5	420
1303	OUT[1013]	-8122.5	290
1304	OUT[1014]	-8141.5	160
1305	OUT[1015]	-8160.5	420
1306	OUT[1016]	-8179.5	290
1307	OUT[1017]	-8198.5	160
1308	OUT[1018]	-8217.5	420
1309	OUT[1019]	-8236.5	290
1310	OUT[1020]	-8255.5	160
1311	OUT[1021]	-8274.5	420
1312	OUT[1022]	-8293.5	290
1313	OUT[1023]	-8312.5	160
1314	OUT[1024]	-8331.5	420
1315	OUT[1025]	-8350.5	290
1316	OUT[1026]	-8369.5	160
1317	OUT[1027]	-8388.5	420
1318	OUT[1028]	-8407.5	290
1319	OUT[1029]	-8426.5	160
1320	OUT[1030]	-8445.5	420
1321	OUT[1031]	-8464.5	290
1322	OUT[1032]	-8483.5	160
1323	OUT[1033]	-8502.5	420
1324	OUT[1034]	-8521.5	290
1325	OUT[1035]	-8540.5	160
1326	OUT[1036]	-8559.5	420
1327	OUT[1037]	-8578.5	290
1328	OUT[1038]	-8597.5	160
1329	OUT[1039]	-8616.5	420
1330	OUT[1040]	-8635.5	290
1331	OUT[1041]	-8654.5	160

1332	OUT[1042]	-8673.5	420
1333	OUT[1043]	-8692.5	290
1334	OUT[1044]	-8711.5	160
1335	OUT[1045]	-8730.5	420
1336	OUT[1046]	-8749.5	290
1337	OUT[1047]	-8768.5	160
1338	OUT[1048]	-8787.5	420
1339	OUT[1049]	-8806.5	290
1340	OUT[1050]	-8825.5	160
1341	OUT[1051]	-8844.5	420
1342	OUT[1052]	-8863.5	290
1343	OUT[1053]	-8882.5	160
1344	OUT[1054]	-8901.5	420
1345	OUT[1055]	-8920.5	290
1346	OUT[1056]	-8939.5	160
1347	OUT[1057]	-8958.5	420
1348	OUT[1058]	-8977.5	290
1349	OUT[1059]	-8996.5	160
1350	OUT[1060]	-9015.5	420
1351	OUT[1061]	-9034.5	290
1352	OUT[1062]	-9053.5	160
1353	OUT[1063]	-9072.5	420
1354	OUT[1064]	-9091.5	290
1355	OUT[1065]	-9110.5	160
1356	OUT[1066]	-9129.5	420
1357	OUT[1067]	-9148.5	290
1358	OUT[1068]	-9167.5	160
1359	OUT[1069]	-9186.5	420
1360	OUT[1070]	-9205.5	290
1361	OUT[1071]	-9224.5	160
1362	OUT[1072]	-9243.5	420
1363	OUT[1073]	-9262.5	290
1364	OUT[1074]	-9281.5	160
1365	OUT[1075]	-9300.5	420
1366	OUT[1076]	-9319.5	290
1367	OUT[1077]	-9338.5	160
1368	OUT[1078]	-9357.5	420
1369	OUT[1079]	-9376.5	290
1370	OUT[1080]	-9395.5	160
1371	OUT[1081]	-9414.5	420
1372	OUT[1082]	-9433.5	290
1373	OUT[1083]	-9452.5	160
1374	OUT[1084]	-9471.5	420
1375	OUT[1085]	-9490.5	290
1376	OUT[1086]	-9509.5	160
1377	OUT[1087]	-9528.5	420
1378	OUT[1088]	-9547.5	290
1379	OUT[1089]	-9566.5	160
1380	OUT[1090]	-9585.5	420
1381	OUT[1091]	-9604.5	290
1382	OUT[1092]	-9623.5	160
1383	OUT[1093]	-9642.5	420
1384	OUT[1094]	-9661.5	290
1385	OUT[1095]	-9680.5	160
1386	OUT[1096]	-9699.5	420
1387	OUT[1097]	-9718.5	290
1388	OUT[1098]	-9737.5	160
1389	OUT[1099]	-9756.5	420
1390	OUT[1100]	-9775.5	290
1391	OUT[1101]	-9794.5	160
1392	OUT[1102]	-9813.5	420
1393	OUT[1103]	-9832.5	290
1394	OUT[1104]	-9851.5	160
1395	OUT[1105]	-9870.5	420
1396	OUT[1106]	-9889.5	290
1397	OUT[1107]	-9908.5	160

1398	OUT[1108]	-9927.5	420
1399	OUT[1109]	-9946.5	290
1400	OUT[1110]	-9965.5	160
1401	OUT[1111]	-9984.5	420
1402	OUT[1112]	-10003.5	290
1403	OUT[1113]	-10022.5	160
1404	OUT[1114]	-10041.5	420
1405	OUT[1115]	-10060.5	290
1406	OUT[1116]	-10079.5	160
1407	OUT[1117]	-10098.5	420
1408	OUT[1118]	-10117.5	290
1409	OUT[1119]	-10136.5	160
1410	OUT[1120]	-10155.5	420
1411	OUT[1121]	-10174.5	290
1412	OUT[1122]	-10193.5	160
1413	OUT[1123]	-10212.5	420
1414	OUT[1124]	-10231.5	290
1415	OUT[1125]	-10250.5	160
1416	OUT[1126]	-10269.5	420
1417	OUT[1127]	-10288.5	290
1418	OUT[1128]	-10307.5	160
1419	OUT[1129]	-10326.5	420
1420	OUT[1130]	-10345.5	290
1421	OUT[1131]	-10364.5	160
1422	OUT[1132]	-10383.5	420
1423	OUT[1133]	-10402.5	290
1424	OUT[1134]	-10421.5	160
1425	OUT[1135]	-10440.5	420
1426	OUT[1136]	-10459.5	290
1427	OUT[1137]	-10478.5	160
1428	OUT[1138]	-10497.5	420
1429	OUT[1139]	-10516.5	290
1430	OUT[1140]	-10535.5	160
1431	OUT[1141]	-10554.5	420
1432	OUT[1142]	-10573.5	290
1433	OUT[1143]	-10592.5	160
1434	OUT[1144]	-10611.5	420
1435	OUT[1145]	-10630.5	290
1436	OUT[1146]	-10649.5	160
1437	OUT[1147]	-10668.5	420
1438	OUT[1148]	-10687.5	290
1439	OUT[1149]	-10706.5	160
1440	OUT[1150]	-10725.5	420
1441	OUT[1151]	-10744.5	290
1442	OUT[1152]	-10763.5	160
1443	OUT[1153]	-10782.5	420
1444	OUT[1154]	-10801.5	290
1445	OUT[1155]	-10820.5	160
1446	OUT[1156]	-10839.5	420
1447	OUT[1157]	-10858.5	290
1448	OUT[1158]	-10877.5	160
1449	OUT[1159]	-10896.5	420
1450	OUT[1160]	-10915.5	290
1451	OUT[1161]	-10934.5	160
1452	OUT[1162]	-10953.5	420
1453	OUT[1163]	-10972.5	290
1454	OUT[1164]	-10991.5	160
1455	OUT[1165]	-11010.5	420
1456	OUT[1166]	-11029.5	290
1457	OUT[1167]	-11048.5	160
1458	OUT[1168]	-11067.5	420
1459	OUT[1169]	-11086.5	290
1460	OUT[1170]	-11105.5	160
1461	OUT[1171]	-11124.5	420
1462	OUT[1172]	-11143.5	290
1463	OUT[1173]	-11162.5	160

1464	OUT[1174]	-11181.5	420
1465	OUT[1175]	-11200.5	290
1466	OUT[1176]	-11219.5	160
1467	OUT[1177]	-11238.5	420
1468	OUT[1178]	-11257.5	290
1469	OUT[1179]	-11276.5	160
1470	OUT[1180]	-11295.5	420
1471	OUT[1181]	-11314.5	290
1472	OUT[1182]	-11333.5	160
1473	OUT[1183]	-11352.5	420
1474	OUT[1184]	-11371.5	290

1475	OUT[1185]	-11390.5	160
1476	OUT[1186]	-11409.5	420
1477	OUT[1187]	-11428.5	290
1478	OUT[1188]	-11447.5	160
1479	OUT[1189]	-11466.5	420
1480	OUT[1190]	-11485.5	290
1481	OUT[1191]	-11504.5	160
1482	OUT[1192]	-11523.5	420
1483	OUT[1193]	-11542.5	290
1484	OUT[1194]	-11561.5	160
1485	OUT[1195]	-11580.5	420

1486	OUT[1196]	-11599.5	290
1487	OUT[1197]	-11618.5	160
1488	OUT[1198]	-11637.5	420
1489	OUT[1199]	-11656.5	290
1490	RPO1	-11717	420
1491	RPO1	-11761	420
1492	RPI1	-11805	420
1493	PASS1	-11849	420
1494	PASS1	-11893	420
1495	DUMMY[35]	-11937	420
1496	OUT[1200]	-11675.5	160

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Data Sheet

NT39207

480/320 Outputs TFT LCD Gate Driver

Version 0.11

Preliminary

1	REVISION HISTORY	3
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Revision History

NT39207 Specification Revision History		
Version	Content	Data
0.0	Original	2005/6/20
0.1	Add power on/off sequence (page 10,11)	2005/6/23
0.2	Modify identification of chip size (page 20)	2005/7/13
0.3	Modify VEE waveform of power sequence (page 10,11) 1*OE to 3*OE (page 7,8) Add pads for MODE,XON & dimension modified (page 20)	2005/8/30
0.4	Modify dummy pins' location & pad size (page 20)	2005/10/18
0.5	Modify Bonding Diagram (page 21)	2005/10/19
0.6	Correct pass line table (page 9) and remove label PWCL (page 14)	2005/12/20
0.7	Add waveforms under IC work with 3-OE. (page 19)	2005/12/23
0.8	Modify alignment mark. (page 20)	2006/01/16
0.9	Modify pass line table (page 9)	2006/04/03
0.10	Modify the definition of "MODE" (page 8)	2006/04/07
0.11	Modify the description of power on/off sequence (page 10)	2007/01/18

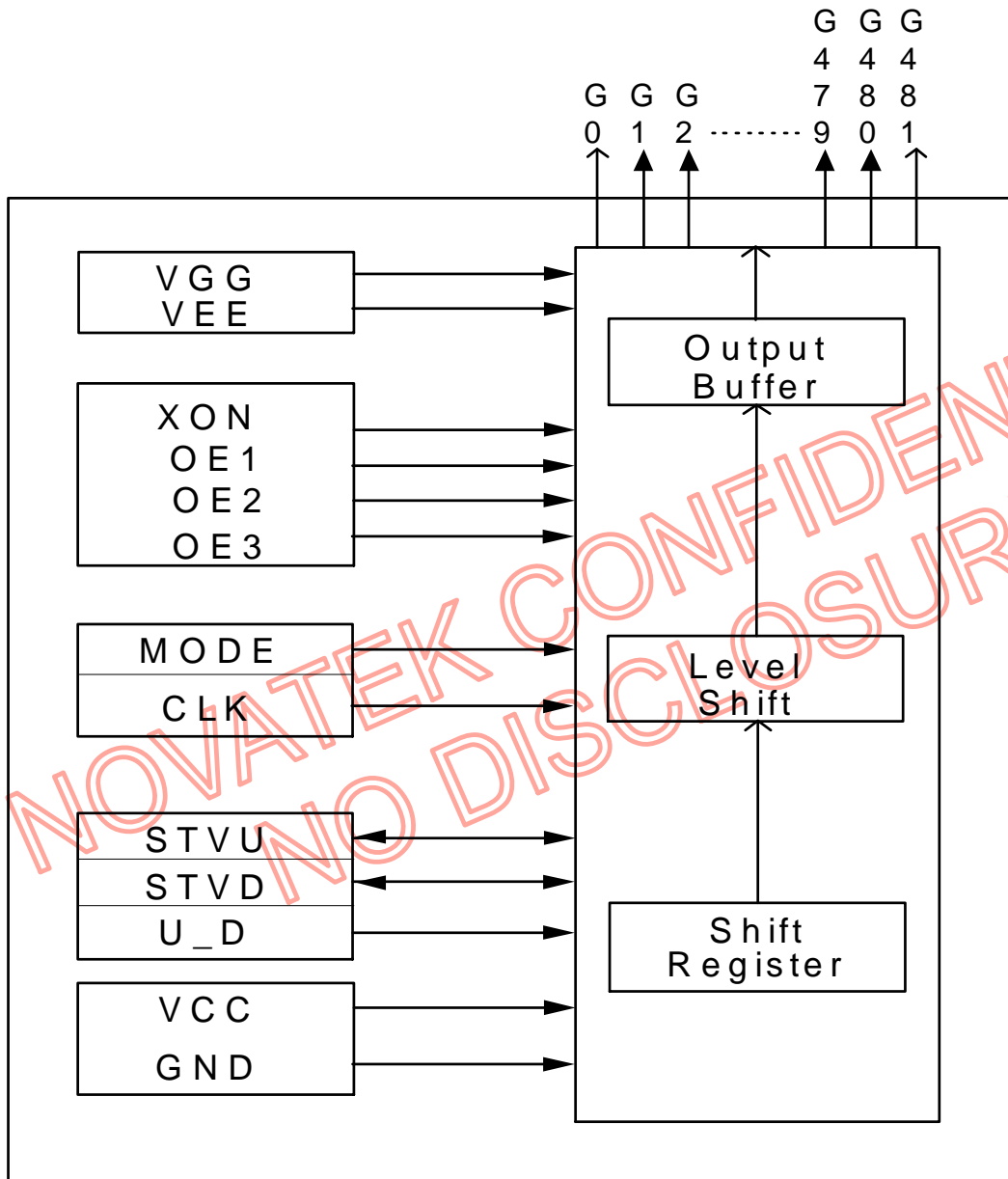
Features

- Gate driver for TFT LCD panel
- 480/320 channel outputs+2pins (Fixed to VEE)
- Bi-directional shift selectable function
- Driving voltage: VEE + 40V
- Double gate scan
- 2.7 ~ 3.6V logical interface
- Cascade function for dot-expansion
- CMOS silicon gate (P-type)
- COG solution

General Description

NT39207 is a dedicated gate driver IC for TFT LCD Panel. After a start pulse is triggered, output pins will output high-driving voltage pulses sequentially for the gate signals of the LCD Panel. This chip also provides shift up/down selection and cascade functions for dot expansion. The special pin location is designed for COG manufacture.

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Block Diagram


Pin Descriptions

Designation	I/O	Descriptions
XONR, XONL	I	Active Low, When XON goes low, all outputs are fixed to VGG. And there is a 200k ohm pull-up resistor with this pin. Xon signal has priority over OE.
OE1R, OE1L	I	Output enabled; these pads are shorted internally; active high. When this pin is applied to "1", the (3n+1) th channel output, n=0, 1, 2, ...159, are disabled (=VEE). This condition will not affect the operation of the internal registers. OE1 control is independent with the CLK. If only use one OE, these OE pins (OE1~3) have to be shorted together.
OE2R, OE2L	I	Output enabled; these pads are shorted internally; active high. When this pin is applied to "1", the (3n+2) th channel output, n=0, 1, 2, ...159, are disabled (=VEE). This condition will not affect the operation of the internal registers. OE2 control is independent with the CLK. If only use one OE, these OE pins (OE1~3) have to be shorted together.
OE3R, OE3L	I	Output enabled; these pads are shorted internally; active high. When this pin is applied to "1", the (3n+3) th channel output, n=0, 1, 2, ...159, are disabled (=VEE). This condition will not affect the operation of the internal registers. OE2 control is independent with the CLK. If only use one OE, these OE pins (OE1~3) have to be shorted together.
U_DR, U_DL	I	Shift up or down control. U_D = "H", up shift: STVD (Input) → G1 ~ G480 → STVU (Output) U_D = "L", down shift: STVU (Input) → G480 ~ G1 → STVD (Output)
CLKR, CLKL	I	Shift clock. Clock signal for internal shift register.
PATHR PATHL	-	Linked together internal.
STVD	I/O	It is an input pin to receive a start pulse when U_D = "1" or an output pin to shift a start pulse to the next stage when U_D = "0". The function is the same as STVU but logical inversion. Please refer to the descriptions of "STVU" and "U_D".
STVU	I/O	It is an input pin when U_D = "0". A "high" pulse is latched at the rising edge of the shift clock, CLK. After a start pulse, a serial pulses are shifted from G480 to G1, and STVD for the next stage. It is an output pin when U_D = "1". A start pulse is shifted for the next stage at the falling edge of the 480th clock of the shift clock.

MODER MODEL	I	Selecting the output mode: 480/320 channels, Normally pull– low . MODE="L": 320 channels (G161~G320 are disabled and fixed to VEE). Default setting is MODE="L" . MODE="H": 480 channels.																																																																																																				
		<table border="1"> <thead> <tr> <th>Output Channel</th> <th>320CH (MODE="L")</th> <th>480CH (MODE="H")</th> <th>320CH OE Control</th> <th>480CH OE Control</th> </tr> </thead> <tbody> <tr><td>G1</td><td>1st</td><td>1st</td><td>OE1</td><td>OE1</td></tr> <tr><td>G2</td><td>2nd</td><td>2nd</td><td>OE2</td><td>OE2</td></tr> <tr><td>G3</td><td>3rd</td><td>3rd</td><td>OE3</td><td>OE3</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>G159</td><td>159th</td><td>159th</td><td>OE3</td><td>OE3</td></tr> <tr><td>G160</td><td>160th</td><td>160th</td><td>OE1</td><td>OE1</td></tr> <tr><td>G161</td><td>Fix to VEE</td><td>161th</td><td>-</td><td>OE2</td></tr> <tr><td>G162</td><td>Fix to VEE</td><td>162th</td><td>-</td><td>OE3</td></tr> <tr><td>G163</td><td>Fix to VEE</td><td>163th</td><td>-</td><td>OE1</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>G318</td><td>Fix to VEE</td><td>318th</td><td>-</td><td>OE3</td></tr> <tr><td>G319</td><td>Fix to VEE</td><td>319th</td><td>-</td><td>OE1</td></tr> <tr><td>G320</td><td>Fix to VEE</td><td>320th</td><td>-</td><td>OE2</td></tr> <tr><td>G321</td><td>161th</td><td>321th</td><td>OE2</td><td>OE3</td></tr> <tr><td>G322</td><td>162th</td><td>322th</td><td>OE3</td><td>OE1</td></tr> <tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr> <tr><td>G478</td><td>318th</td><td>478th</td><td>OE3</td><td>OE1</td></tr> <tr><td>G479</td><td>319th</td><td>479th</td><td>OE1</td><td>OE2</td></tr> <tr><td>G480</td><td>320th</td><td>480th</td><td>OE2</td><td>OE3</td></tr> </tbody> </table>	Output Channel	320CH (MODE="L")	480CH (MODE="H")	320CH OE Control	480CH OE Control	G1	1 st	1 st	OE1	OE1	G2	2 nd	2 nd	OE2	OE2	G3	3 rd	3 rd	OE3	OE3	:	:	:	:	:	G159	159 th	159 th	OE3	OE3	G160	160 th	160 th	OE1	OE1	G161	Fix to VEE	161 th	-	OE2	G162	Fix to VEE	162 th	-	OE3	G163	Fix to VEE	163 th	-	OE1	:	:	:	:	:	G318	Fix to VEE	318 th	-	OE3	G319	Fix to VEE	319 th	-	OE1	G320	Fix to VEE	320 th	-	OE2	G321	161 th	321 th	OE2	OE3	G322	162 th	322 th	OE3	OE1	:	:	:	:	:	G478	318 th	478 th	OE3	OE1	G479	319 th	479 th	OE1	OE2	G480	320 th	480 th	OE2	OE3
		Output Channel	320CH (MODE="L")	480CH (MODE="H")	320CH OE Control	480CH OE Control																																																																																																
		G1	1 st	1 st	OE1	OE1																																																																																																
		G2	2 nd	2 nd	OE2	OE2																																																																																																
		G3	3 rd	3 rd	OE3	OE3																																																																																																
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		G159	159 th	159 th	OE3	OE3																																																																																																
		G160	160 th	160 th	OE1	OE1																																																																																																
		G161	Fix to VEE	161 th	-	OE2																																																																																																
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		:	:	:	:	:																																																																																																
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G479	319 th	479 th	OE1	OE2																																																																																																		
G480	320 th	480 th	OE2	OE3																																																																																																		
VGGR, VGGL	PI	Positive power supply for G1 ~ G480 outputs																																																																																																				
VEER, VEEL	PI	Negative power supply for G0 ~ G481 outputs																																																																																																				
VCCR, VCCL	PI	Power supply for digital circuit.																																																																																																				
GNDR, GNDL	PI	Ground pin																																																																																																				
G1 ~ G480	O	For driving LCD's gate signals, the output amplitude of these pins is VGG - VEE. Output timing of these signals is synchronous with the rising edge of shift clock.																																																																																																				
G0, G481	O	LCD panel auxiliary pins. Regardless of shift data, these pins output VEE level.																																																																																																				

- I : Input, O : Output, P : Power, D : Dummy, S : Shorted line, M : Mark, PI : Power input, PO : Power output, T : For testing, I/O : Input / Output. PS: Power Setting, C: Capacitor pin.
- U_DL = U/DL , U_DR = U/DR , U_D=U/D

Pass line pin name

Pass Line No	Pad Name	
1	XONR	XONL
2	OE1R	OE1L
3	OE2R	OE2L
4	OE3R	OE3L
5	U_DR	U_DL
6	CLKR	CLKL
7	PATHR	PATHL
8	VGGR	VGGL
9	VCCR	VCCL
10	MODER	MODEL
11	VEER	VEEL

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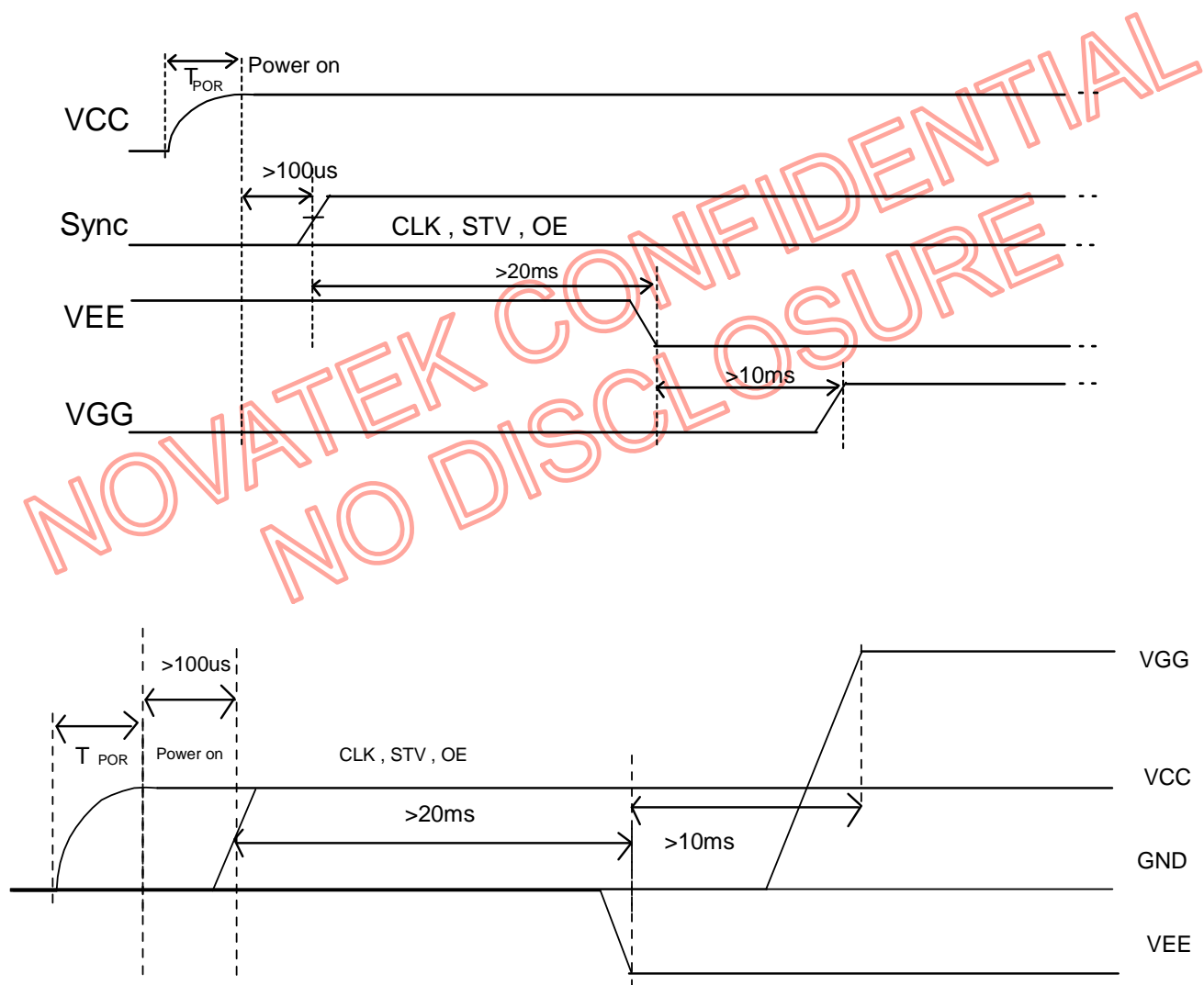
Functional Description

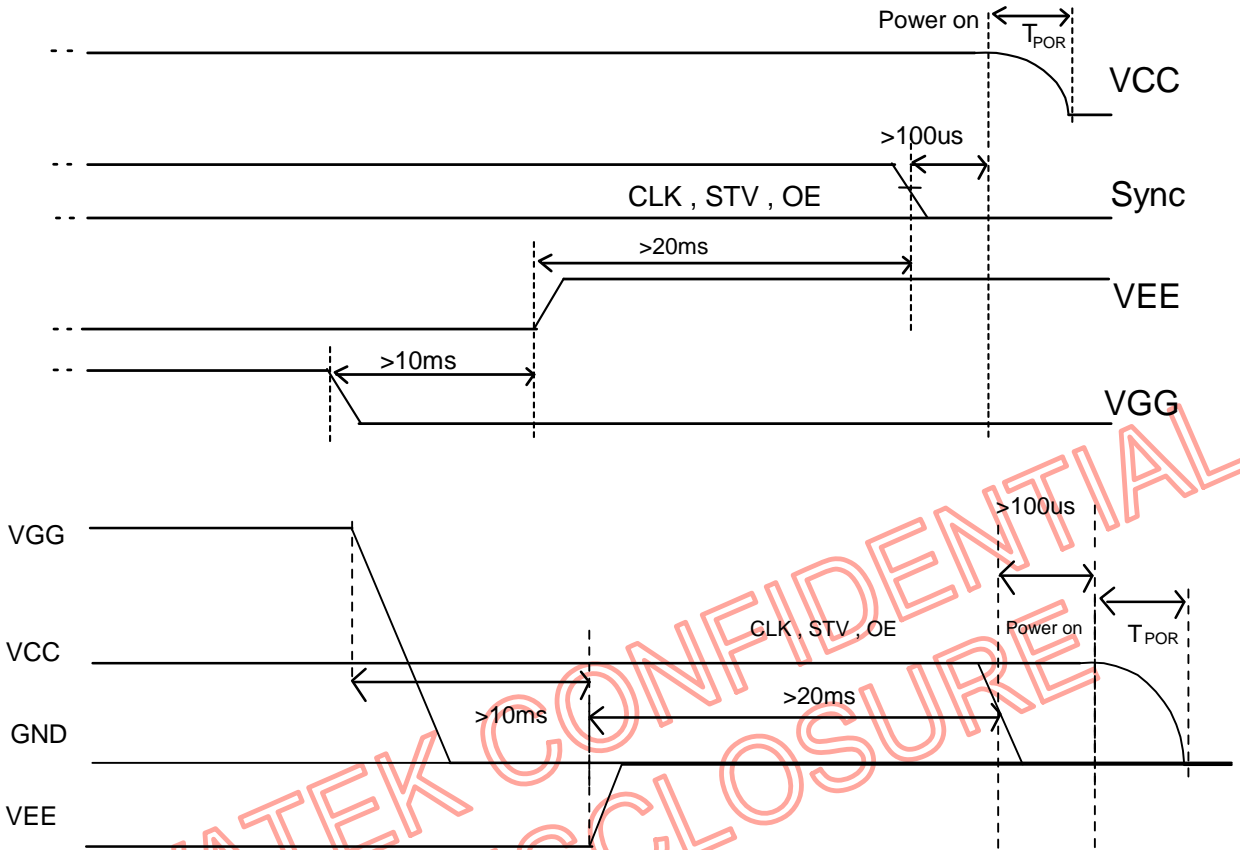
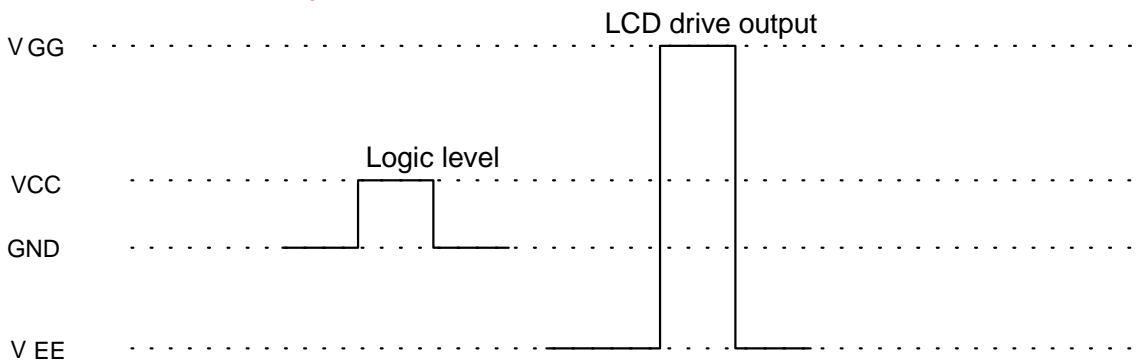
1. Power on/off sequence:

This IC is a high-voltage LCD driver, so it may be damaged by a large current flow if an incorrect power sequence is used. A recommended sequence is to connect the drive powers ,VEE & VGG , after the initialization of logic power, VCC.

For power-off sequence , either turning off logic system after shutting off the drive power or turning off all power simultaneously at the same time are suggested.

■ Power on sequence



■ Power off sequence

2. Power level:


Note: For the input signals: CLK, XON, OE, U_D, STVD & STVU, MODE, "High" level=VCC, "Low" level=GND

Absolute Maximum Rating*

Logic supply voltage, VCC	- 0.3V to +6V
Supply voltage, VGG	- 0.3V to +40V
Supply voltage, VEE	- 20V to +0.3V
Supply range, VGG-VEE	- 0.3V to +40V
Operating temperature	-30 °C to 85 °C
Storage temperature	-55 °C to 125 °C

***Comments**

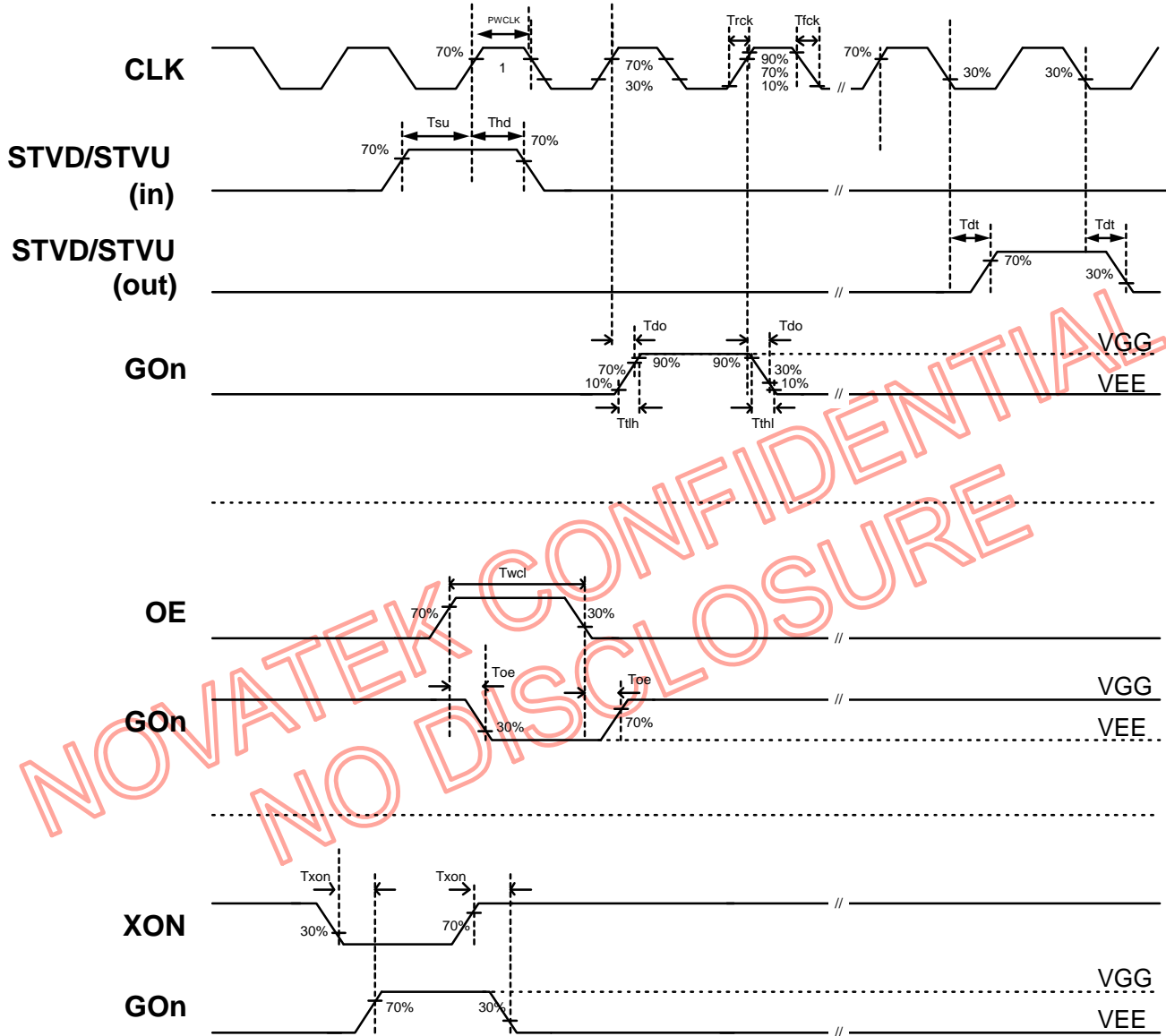
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
VGG	VGG Voltage	7	-	VEE +40	V	
VEE	VEE Voltage	-20	-	-5	V	
Vxo	Voltage Range of VGG - VEE	12	-	40	V	VCC = 3.3V
VCC	VCC Supplied Voltage	2.7	3.3	3.6	V	
VIH	High Level Input Voltage	0.7 X VCC	-	VCC	V	VCC = 3.3V
VIL	Low Level Input Voltage	0	-	0.3 X VCC	V	VCC = 3.3V
IXOH	High Level Output Current	0.5	-	-	mA	Driving current, VO = VGG -0.5V
IXOL	Low Level Output Current	-0.5	-	-	mA	Sink current, VO = VEE + 0.5V
IPOH	High Level Output Current	200	-	-	uA	STVD/STVU, VO = VCC - 0.3V
IPOL	Low Level Output Current	-200	-	-	uA	STVD/STVU, VO = 0.3V
Rin	Pull-up Impedance	70K	200K	-	ohm	XON , MODER,MODEL
IIL	Input Leakage Current	-	-	± 1	uA	Except XON & MODER,MODEL
ICC	Operating Current Consumption	-	-	50	uA	VCC=3.3V, Fclk=20KHz, No load
IGG	Operating Current Consumption	-	-	100	uA	VGG=25V, Fclk=20KHz, No load
IEE	Operating Current Consumption	-	-	-100	uA	VEE=-15V, Fclk=20KHz, No load

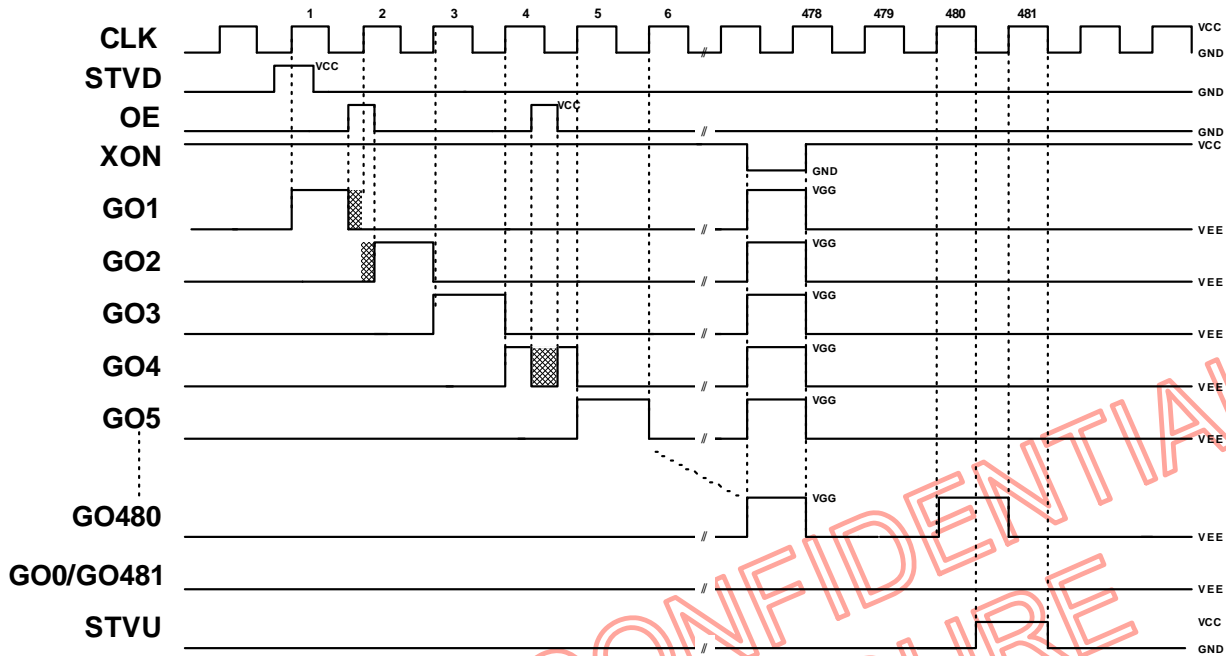
AC Characteristics (VGG=25V, VEE=-15V, VCC=3.3V, GND=0V, TA= 25 °C)

Symbol	Parameters	Min.	Typ.	Max.	Unit	Conditions
Tdt	STVD/STVU Delay Time	-	-	500	ns	CL = 20pF
Tdo	Driver Output Delay Time	-	-	900	ns	CL = 220pF
Tthl	Output Falling Time	-	400	800	ns	CL = 220pF, 90% to 10%
Tthh	Output Rise Time	-	500	1000	ns	CL = 220pF, 10% to 90%
Txon	XON to Driver Output Delay Time	-	-	10	us	CL = 220pF
Toe	OE to Driver Output Delay Time	-	-	900	ns	CL = 220pF
Fclk	Clock Frequency	-	-	200	KHz	In cascade connection
Trck	Clock Rise Time	-	-	100	ns	CL = 20pF
Tfck	Clock Falling Time	-	-	100	ns	CL = 20pF
PWCLK	Clock Pulse Width (High period or Low period)	500	-	-	ns	
Tsu	STVD/STVU Set-up Time	200	-	-	ns	
Thd	STVD/STVU Hold Time	300	-	-	ns	
Twcl	Output Enabled pulse width	1	-	-	us	
T _{POR}	Power-On Reset slew time	-	-	5	ms	From 0V to 90% VCC

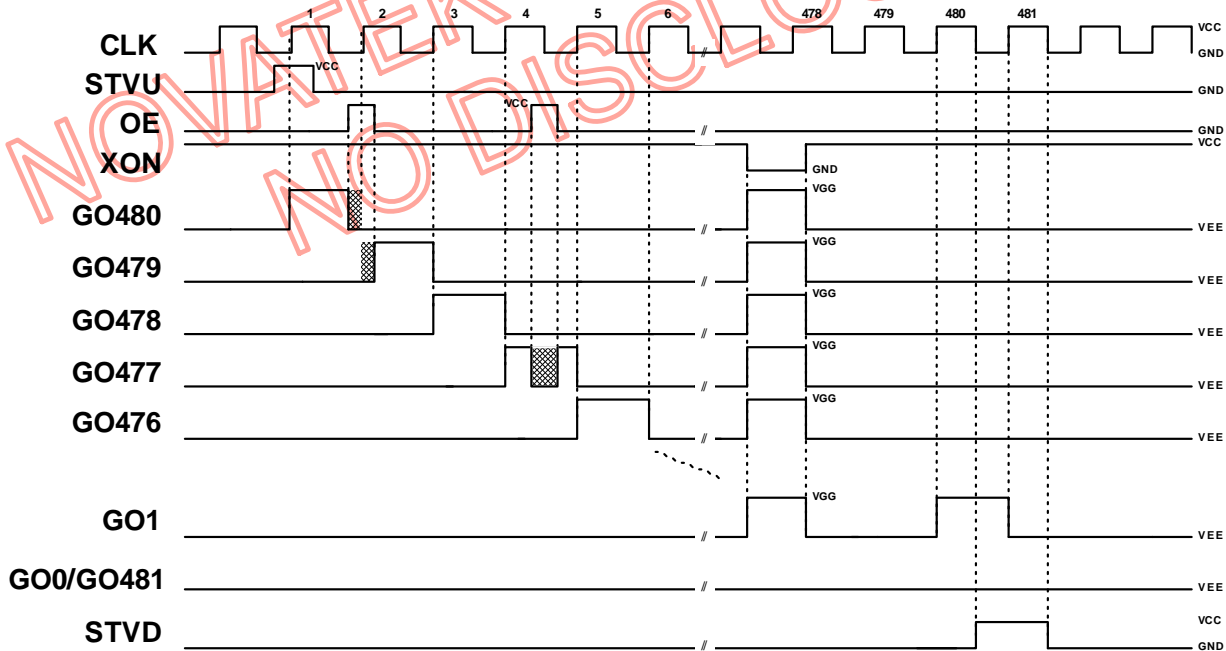
Timing Waveforms


Operation(Single-pulse)

1. U/D = "H"

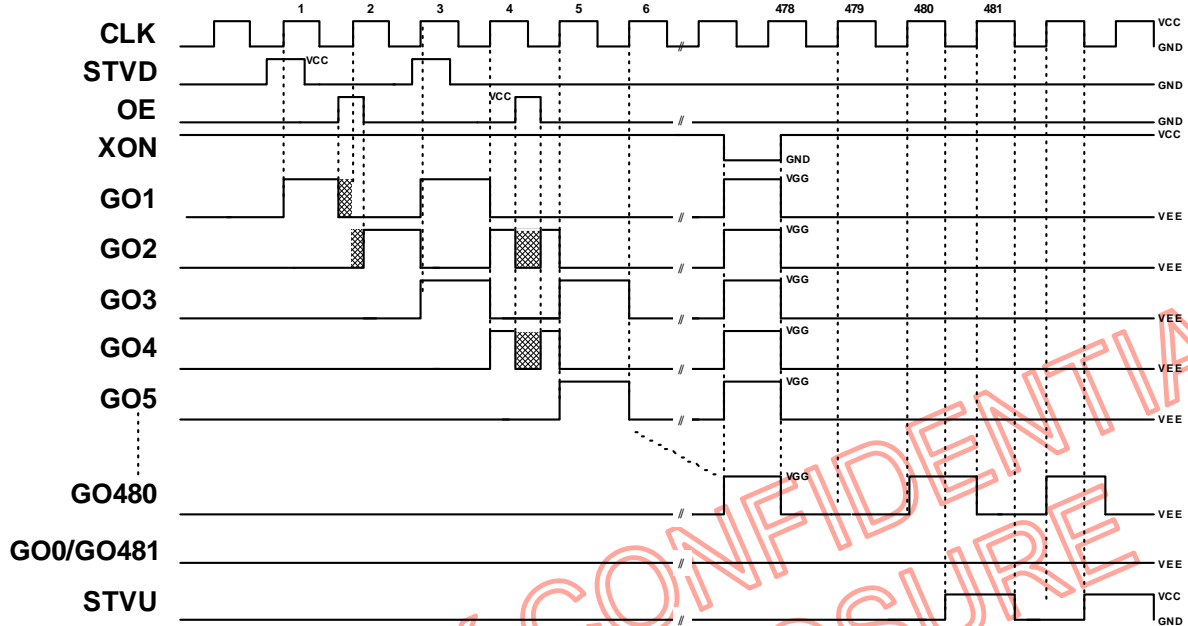


2. U/D = "L"

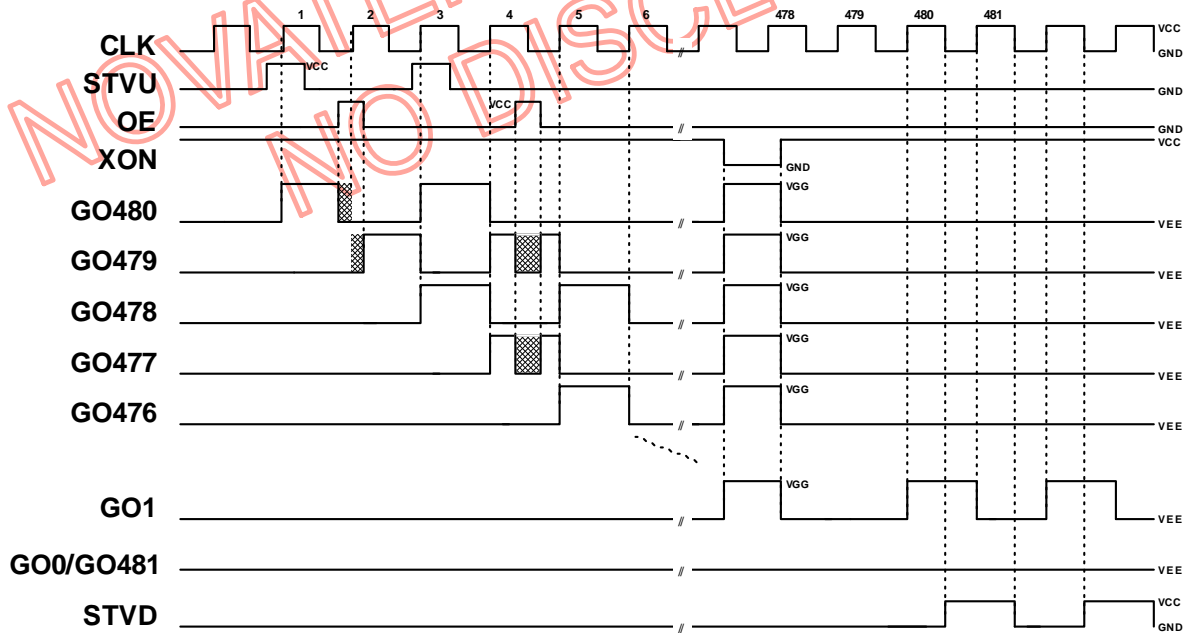


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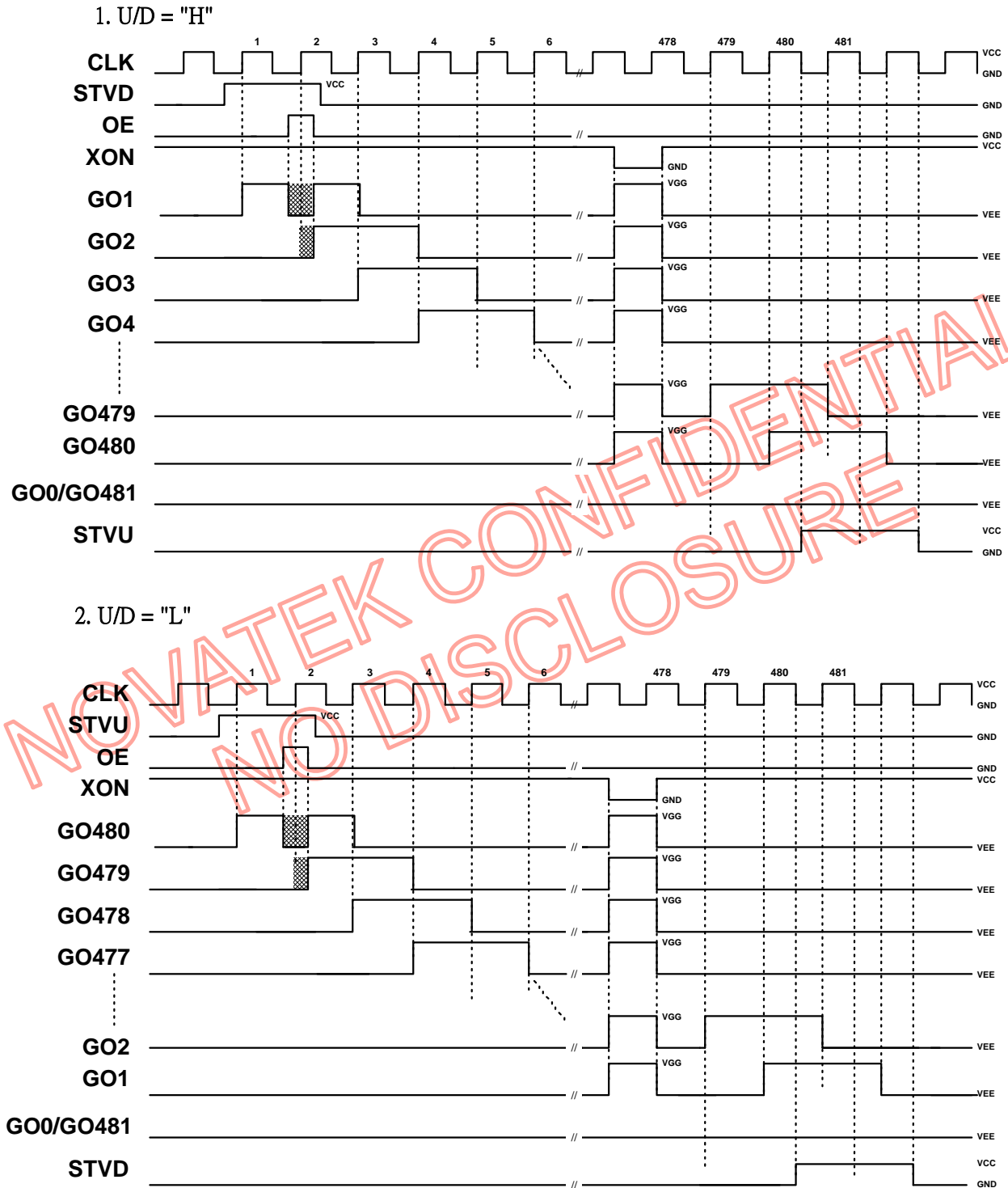
Operation(Double-pulse)

1. U/D = "H"



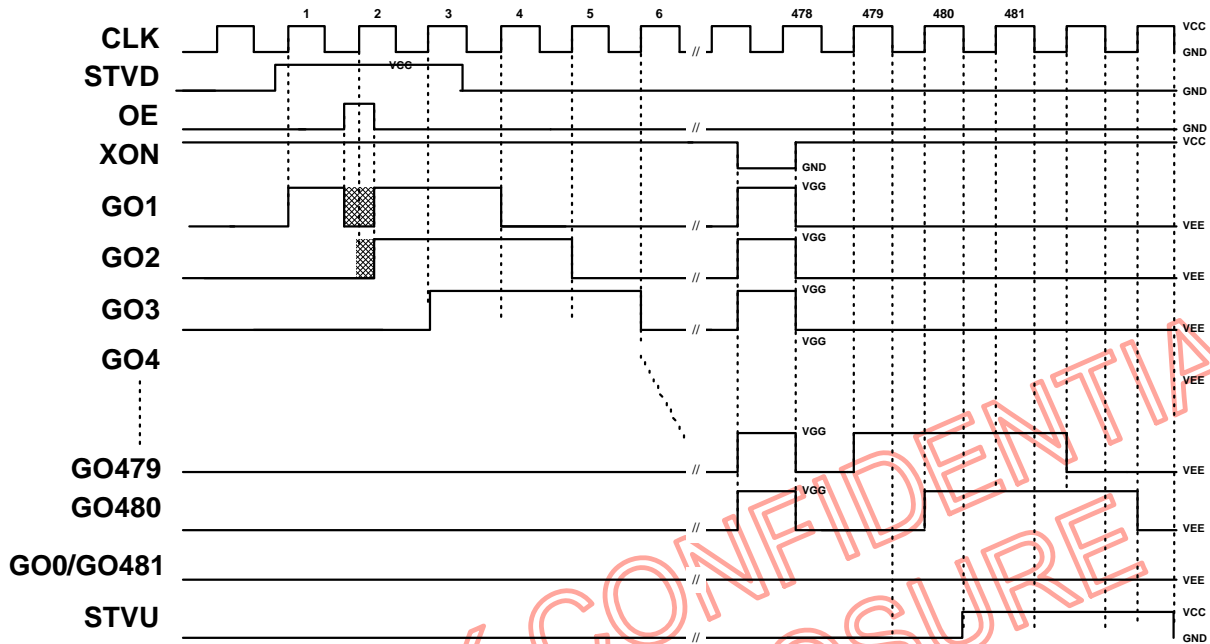
2. U/D = "L"


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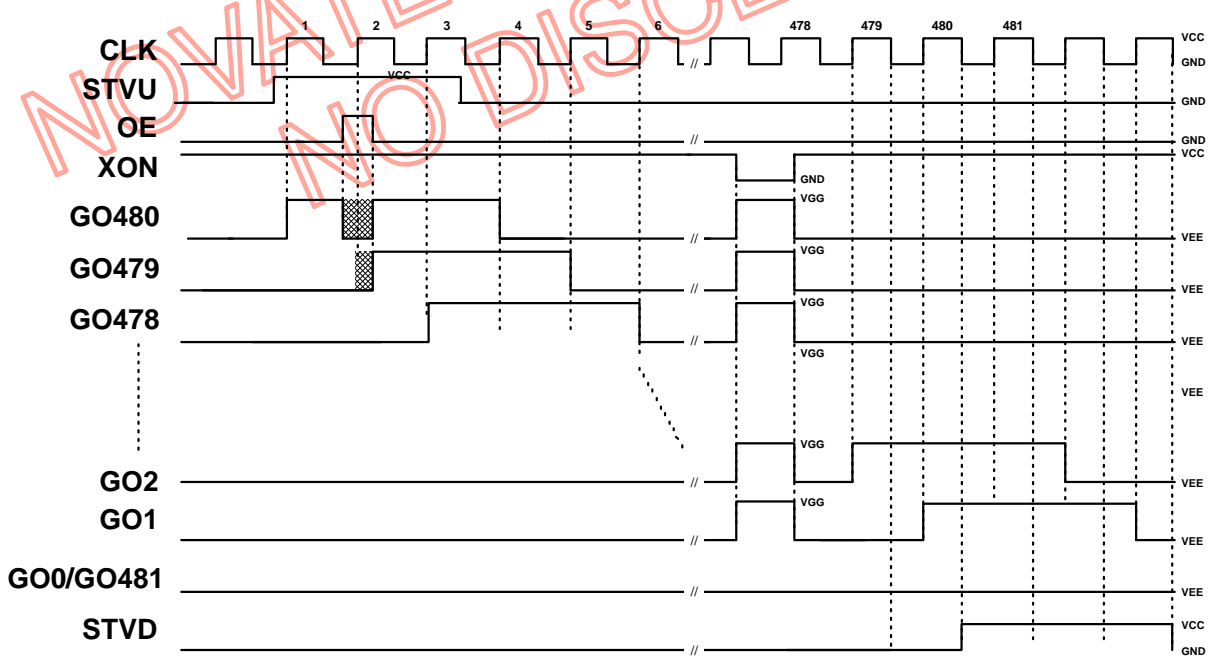
Operation(long start pulse)(2CKV)


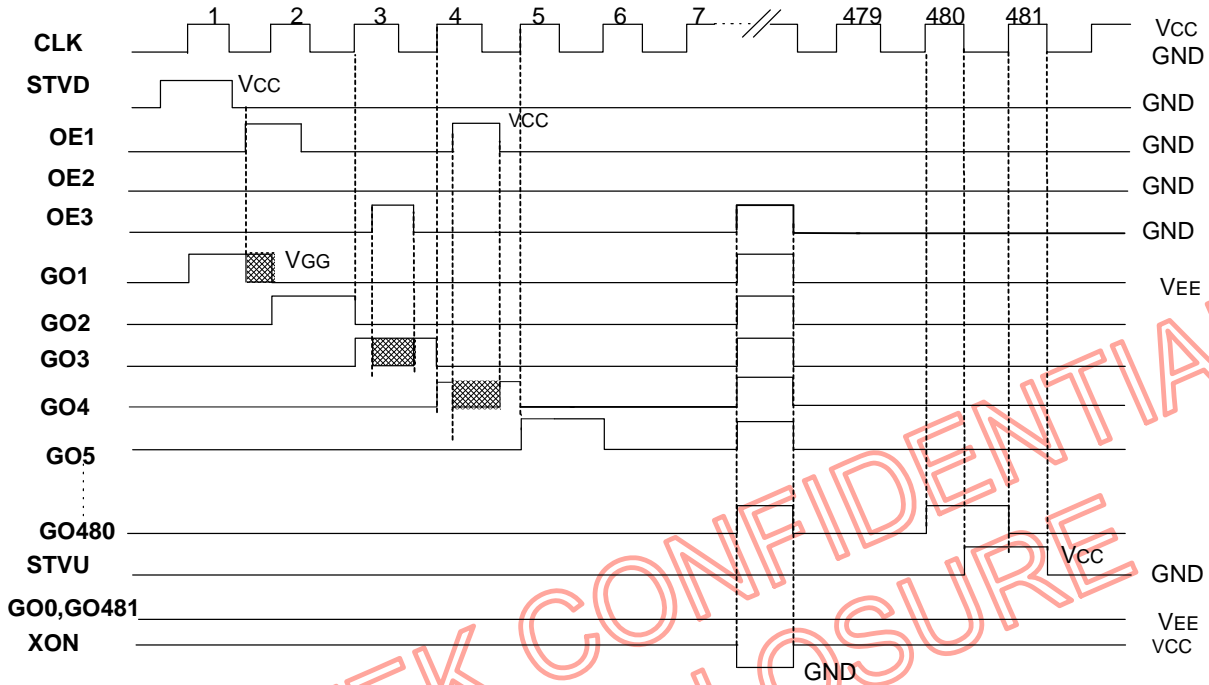
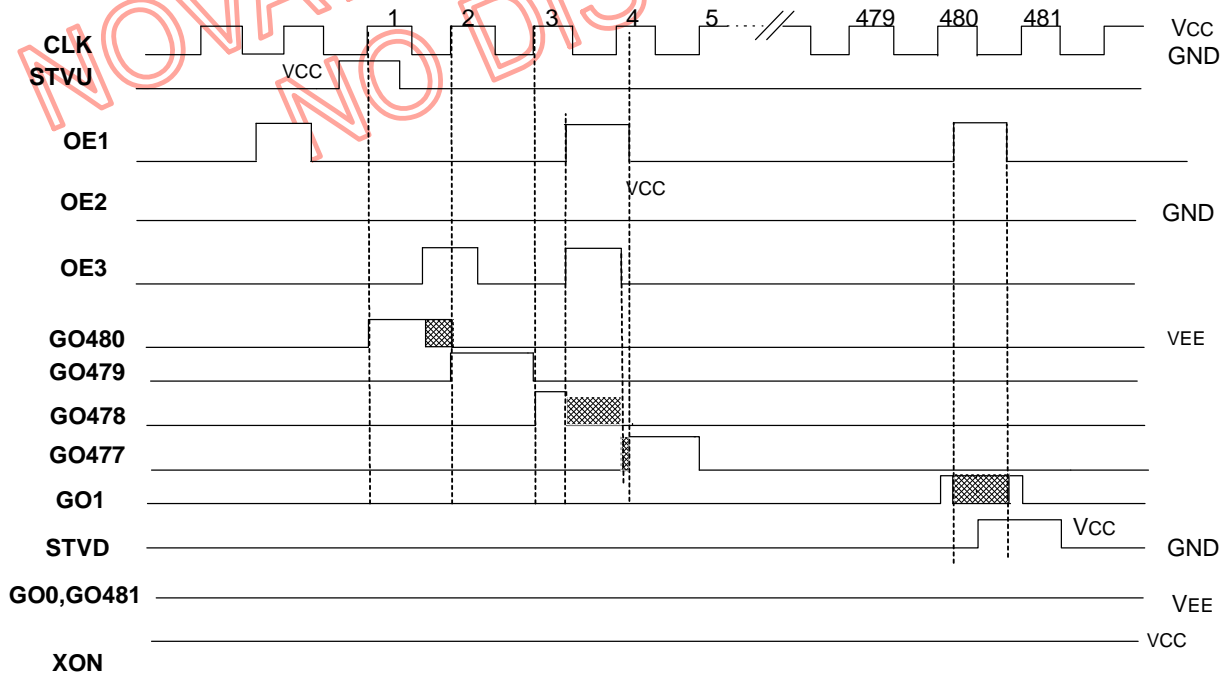
Operation(long start pulse)(3CKV)


1. U/D = "H"

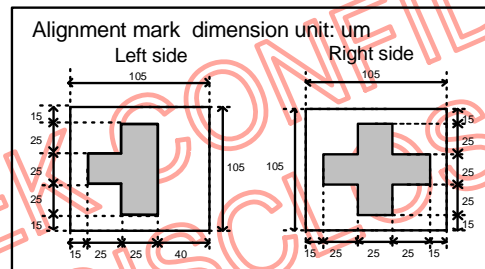
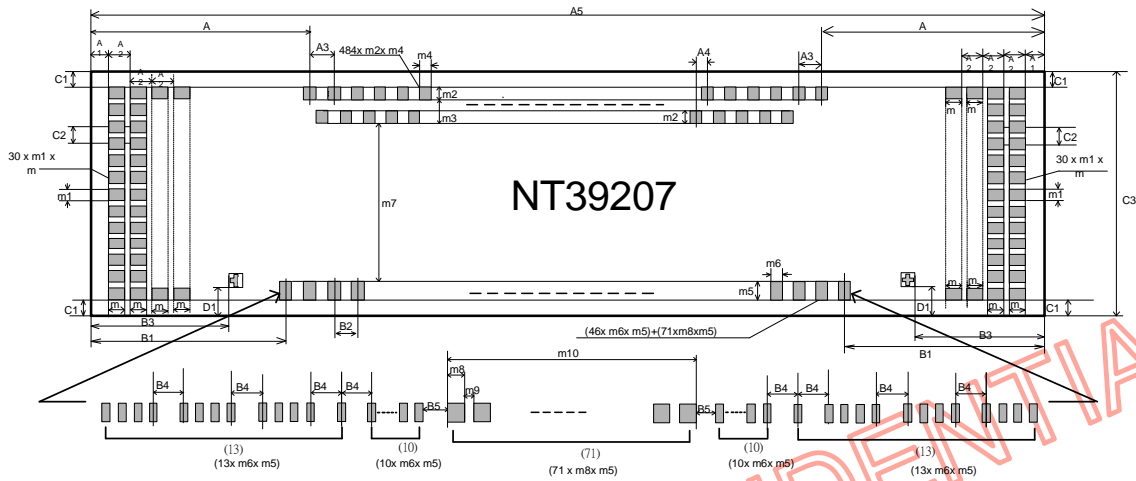


2. U/D = "L"


 : Deleted from normal output by OE

Operation(3 OE)
1. U_D = 'H'

2. U_D = 'L'


 : Deleted from normal output by OEx

Chip Outline Dimensions


Symbol	Dimensions in μm	Symbol	Dimensions in μm
A	710	D1	105
A1	70	m	50
A2	65	m1	45
A3	50	m2	84
A4	25	m3	119
A5	13520	m4	25
B1	666	m5	85
B2	52	m6	40
B3	440	m7	609
B4	80	m8	105
B5	40.5	m9	30
C1	70	m10	9555
C2	71		
C3	1037		

Bonding Diagram

No.	TextName	CX	CY
1	XONL	-6665	426
2	XONL	-6600	426
3	XONL	-6535	426
4	XONL	-6470	426
5	OE1L	-6665	355
6	OE1L	-6600	355
7	OE2L	-6665	284
8	OE2L	-6600	284
9	OE3L	-6665	213
10	OE3L	-6600	213
11	U/DL	-6665	142
12	U/DL	-6600	142
13	CLKL	-6665	71
14	CLKL	-6600	71
15	PATHL	-6665	0
16	PATHL	-6600	0
17	STVU	-6665	-71
18	STVU	-6600	-71
19	VGGL	-6665	-142
20	VGGL	-6600	-142
21	VGGL	-6665	-213
22	VGGL	-6600	-213
23	VCCL	-6665	-284
24	VCCL	-6600	-284
25	VCCL	-6665	-355
26	VCCL	-6600	-355
27	MODEL	-6665	-426
28	MODEL	-6600	-426
29	MODEL	-6535	-426
30	MODEL	-6470	-426
31	VEEL	-6094	-406
32	VEEL	-6042	-406
33	VEEL	-5990	-406
34	VEEL	-5938	-406
35	VGGL	-5858	-406
36	VGGL	-5806	-406
37	VGGL	-5754	-406
38	VGGL	-5702	-406
39	VCCL	-5622	-406
40	VCCL	-5570	-406

No.	TextName	CX	CY
41	VCCL	-5518	-406
42	VCCL	-5466	-406
43	MODEL	-5386	-406
44	GNDL	-5306	-406
45	GNDL	-5254	-406
46	GNDL	-5202	-406
47	GNDL	-5150	-406
48	GNDL	-5098	-406
49	GNDL	-5046	-406
50	GNDL	-4994	-406
51	GNDL	-4942	-406
52	GNDL	-4890	-406
53	GNDL	-4838	-406
54	DUMMY[1]	-4725	-406
55	DUMMY[2]	-4590	-406
56	DUMMY[3]	-4455	-406
57	DUMMY[4]	-4320	-406
58	DUMMY[5]	-4185	-406
59	DUMMY[6]	-4050	-406
60	DUMMY[7]	-3915	-406
61	DUMMY[8]	-3780	-406
62	DUMMY[9]	-3645	-406
63	DUMMY[10]	-3510	-406
64	DUMMY[11]	-3375	-406
65	DUMMY[12]	-3240	-406
66	DUMMY[13]	-3105	-406
67	DUMMY[14]	-2970	-406
68	DUMMY[15]	-2835	-406
69	DUMMY[16]	-2700	-406
70	DUMMY[17]	-2565	-406
71	DUMMY[18]	-2430	-406
72	DUMMY[19]	-2295	-406
73	DUMMY[20]	-2160	-406
74	DUMMY[21]	-2025	-406
75	DUMMY[22]	-1890	-406
76	DUMMY[23]	-1755	-406
77	DUMMY[24]	-1620	-406
78	DUMMY[25]	-1485	-406
79	DUMMY[26]	-1350	-406
80	DUMMY[27]	-1215	-406

No.	TextName	CX	CY
81	DUMMY[28]	-1080	-406
82	DUMMY[29]	-945	-406
83	DUMMY[30]	-810	-406
84	DUMMY[31]	-675	-406
85	DUMMY[32]	-540	-406
86	DUMMY[33]	-405	-406
87	DUMMY[34]	-270	-406
88	DUMMY[35]	-135	-406
89	DUMMY[36]	0	-406
90	DUMMY[37]	135	-406
91	DUMMY[38]	270	-406
92	DUMMY[39]	405	-406
93	DUMMY[40]	540	-406
94	DUMMY[41]	675	-406
95	DUMMY[42]	810	-406
96	DUMMY[43]	945	-406
97	DUMMY[44]	1080	-406
98	DUMMY[45]	1215	-406
99	DUMMY[46]	1350	-406
100	DUMMY[47]	1485	-406
101	DUMMY[48]	1620	-406
102	DUMMY[49]	1755	-406
103	DUMMY[50]	1890	-406
104	DUMMY[51]	2025	-406
105	DUMMY[52]	2160	-406
106	DUMMY[53]	2295	-406
107	DUMMY[54]	2430	-406
108	DUMMY[55]	2565	-406
109	DUMMY[56]	2700	-406
110	DUMMY[57]	2835	-406
111	DUMMY[58]	2970	-406
112	DUMMY[59]	3105	-406
113	DUMMY[60]	3240	-406
114	DUMMY[61]	3375	-406
115	DUMMY[62]	3510	-406
116	DUMMY[63]	3645	-406
117	DUMMY[64]	3780	-406
118	DUMMY[65]	3915	-406
119	DUMMY[66]	4050	-406
120	DUMMY[67]	4185	-406

No.	TextName	CX	CY
121	DUMMY[68]	4320	-406
122	DUMMY[69]	4455	-406
123	DUMMY[70]	4590	-406
124	DUMMY[71]	4725	-406
125	GNDR	4838	-406
126	GNDR	4890	-406
127	GNDR	4942	-406
128	GNDR	4994	-406
129	GNDR	5046	-406
130	GNDR	5098	-406
131	GNDR	5150	-406
132	GNDR	5202	-406
133	GNDR	5254	-406
134	GNDR	5306	-406
135	MODER	5386	-406
136	VCCR	5622	-406
137	VCCR	5570	-406
138	VCCR	5518	-406
139	VCCR	5466	-406
140	VGGR	5858	-406
141	VGGR	5806	-406
142	VGGR	5754	-406
143	VGGR	5702	-406
144	VEER	6094	-406
145	VEER	6042	-406
146	VEER	5990	-406
147	VEER	5938	-406
148	MODER	6470	-426
149	MODER	6535	-426
150	MODER	6600	-426
151	MODER	6665	-426
152	VCCR	6665	-355
153	VCCR	6600	-355
154	VCCR	6665	-284
155	VCCR	6600	-284
156	VGGR	6665	-213
157	VGGR	6600	-213
158	VGGR	6665	-142
159	VGGR	6600	-142
160	STVD	6665	-71

No.	TextName	CX	CY
161	STVD	6600	-71
162	PATHR	6665	0
163	PATHR	6600	0
164	CLKR	6665	71
165	CLKR	6600	71
166	U/DR	6665	142
167	U/DR	6600	142
168	OE3R	6665	213
169	OE3R	6600	213
170	OE2R	6665	284
171	OE2R	6600	284
172	OE1R	6665	355
173	OE1R	6600	355
174	XONR	6665	426
175	XONR	6600	426
176	XONR	6535	426
177	XONR	6470	426
178	DUMMY[72]	6050	406.5
179	G[0]	6000	406.5
180	G[1]	5975	287.5
181	G[2]	5950	406.5
182	G[3]	5925	287.5
183	G[4]	5900	406.5
184	G[5]	5875	287.5
185	G[6]	5850	406.5
186	G[7]	5825	287.5
187	G[8]	5800	406.5
188	G[9]	5775	287.5
189	G[10]	5750	406.5
190	G[11]	5725	287.5
191	G[12]	5700	406.5
192	G[13]	5675	287.5
193	G[14]	5650	406.5
194	G[15]	5625	287.5
195	G[16]	5600	406.5
196	G[17]	5575	287.5
197	G[18]	5550	406.5
198	G[19]	5525	287.5
199	G[20]	5500	406.5
200	G[21]	5475	287.5

No.	TextName	CX	CY
201	G[22]	5450	406.5
202	G[23]	5425	287.5
203	G[24]	5400	406.5
204	G[25]	5375	287.5
205	G[26]	5350	406.5
206	G[27]	5325	287.5
207	G[28]	5300	406.5
208	G[29]	5275	287.5
209	G[30]	5250	406.5
210	G[31]	5225	287.5
211	G[32]	5200	406.5
212	G[33]	5175	287.5
213	G[34]	5150	406.5
214	G[35]	5125	287.5
215	G[36]	5100	406.5
216	G[37]	5075	287.5
217	G[38]	5050	406.5
218	G[39]	5025	287.5
219	G[40]	5000	406.5
220	G[41]	4975	287.5
221	G[42]	4950	406.5
222	G[43]	4925	287.5
223	G[44]	4900	406.5
224	G[45]	4875	287.5
225	G[46]	4850	406.5
226	G[47]	4825	287.5
227	G[48]	4800	406.5
228	G[49]	4775	287.5
229	G[50]	4750	406.5
230	G[51]	4725	287.5
231	G[52]	4700	406.5
232	G[53]	4675	287.5
233	G[54]	4650	406.5
234	G[55]	4625	287.5
235	G[56]	4600	406.5
236	G[57]	4575	287.5
237	G[58]	4550	406.5
238	G[59]	4525	287.5
239	G[60]	4500	406.5
240	G[61]	4475	287.5

No.	TextName	CX	CY
241	G[62]	4450	406.5
242	G[63]	4425	287.5
243	G[64]	4400	406.5
244	G[65]	4375	287.5
245	G[66]	4350	406.5
246	G[67]	4325	287.5
247	G[68]	4300	406.5
248	G[69]	4275	287.5
249	G[70]	4250	406.5
250	G[71]	4225	287.5
251	G[72]	4200	406.5
252	G[73]	4175	287.5
253	G[74]	4150	406.5
254	G[75]	4125	287.5
255	G[76]	4100	406.5
256	G[77]	4075	287.5
257	G[78]	4050	406.5
258	G[79]	4025	287.5
259	G[80]	4000	406.5
260	G[81]	3975	287.5
261	G[82]	3950	406.5
262	G[83]	3925	287.5
263	G[84]	3900	406.5
264	G[85]	3875	287.5
265	G[86]	3850	406.5
266	G[87]	3825	287.5
267	G[88]	3800	406.5
268	G[89]	3775	287.5
269	G[90]	3750	406.5
270	G[91]	3725	287.5
271	G[92]	3700	406.5
272	G[93]	3675	287.5
273	G[94]	3650	406.5
274	G[95]	3625	287.5
275	G[96]	3600	406.5
276	G[97]	3575	287.5
277	G[98]	3550	406.5
278	G[99]	3525	287.5
279	G[100]	3500	406.5
280	G[101]	3475	287.5

No.	TextName	CX	CY
281	G[102]	3450	406.5
282	G[103]	3425	287.5
283	G[104]	3400	406.5
284	G[105]	3375	287.5
285	G[106]	3350	406.5
286	G[107]	3325	287.5
287	G[108]	3300	406.5
288	G[109]	3275	287.5
289	G[110]	3250	406.5
290	G[111]	3225	287.5
291	G[112]	3200	406.5
292	G[113]	3175	287.5
293	G[114]	3150	406.5
294	G[115]	3125	287.5
295	G[116]	3100	406.5
296	G[117]	3075	287.5
297	G[118]	3050	406.5
298	G[119]	3025	287.5
299	G[120]	3000	406.5
300	G[121]	2975	287.5
301	G[122]	2950	406.5
302	G[123]	2925	287.5
303	G[124]	2900	406.5
304	G[125]	2875	287.5
305	G[126]	2850	406.5
306	G[127]	2825	287.5
307	G[128]	2800	406.5
308	G[129]	2775	287.5
309	G[130]	2750	406.5
310	G[131]	2725	287.5
311	G[132]	2700	406.5
312	G[133]	2675	287.5
313	G[134]	2650	406.5
314	G[135]	2625	287.5
315	G[136]	2600	406.5
316	G[137]	2575	287.5
317	G[138]	2550	406.5
318	G[139]	2525	287.5
319	G[140]	2500	406.5
320	G[141]	2475	287.5

No.	TextName	CX	CY
321	G[142]	2450	406.5
322	G[143]	2425	287.5
323	G[144]	2400	406.5
324	G[145]	2375	287.5
325	G[146]	2350	406.5
326	G[147]	2325	287.5
327	G[148]	2300	406.5
328	G[149]	2275	287.5
329	G[150]	2250	406.5
330	G[151]	2225	287.5
331	G[152]	2200	406.5
332	G[153]	2175	287.5
333	G[154]	2150	406.5
334	G[155]	2125	287.5
335	G[156]	2100	406.5
336	G[157]	2075	287.5
337	G[158]	2050	406.5
338	G[159]	2025	287.5
339	G[160]	2000	406.5
340	G[161]	1975	287.5
341	G[162]	1950	406.5
342	G[163]	1925	287.5
343	G[164]	1900	406.5
344	G[165]	1875	287.5
345	G[166]	1850	406.5
346	G[167]	1825	287.5
347	G[168]	1800	406.5
348	G[169]	1775	287.5
349	G[170]	1750	406.5
350	G[171]	1725	287.5
351	G[172]	1700	406.5
352	G[173]	1675	287.5
353	G[174]	1650	406.5
354	G[175]	1625	287.5
355	G[176]	1600	406.5
356	G[177]	1575	287.5
357	G[178]	1550	406.5
358	G[179]	1525	287.5
359	G[180]	1500	406.5
360	G[181]	1475	287.5

No.	TextName	CX	CY
361	G[182]	1450	406.5
362	G[183]	1425	287.5
363	G[184]	1400	406.5
364	G[185]	1375	287.5
365	G[186]	1350	406.5
366	G[187]	1325	287.5
367	G[188]	1300	406.5
368	G[189]	1275	287.5
369	G[190]	1250	406.5
370	G[191]	1225	287.5
371	G[192]	1200	406.5
372	G[193]	1175	287.5
373	G[194]	1150	406.5
374	G[195]	1125	287.5
375	G[196]	1100	406.5
376	G[197]	1075	287.5
377	G[198]	1050	406.5
378	G[199]	1025	287.5
379	G[200]	1000	406.5
380	G[201]	975	287.5
381	G[202]	950	406.5
382	G[203]	925	287.5
383	G[204]	900	406.5
384	G[205]	875	287.5
385	G[206]	850	406.5
386	G[207]	825	287.5
387	G[208]	800	406.5
388	G[209]	775	287.5
389	G[210]	750	406.5
390	G[211]	725	287.5
391	G[212]	700	406.5
392	G[213]	675	287.5
393	G[214]	650	406.5
394	G[215]	625	287.5
395	G[216]	600	406.5
396	G[217]	575	287.5
397	G[218]	550	406.5
398	G[219]	525	287.5
399	G[220]	500	406.5
400	G[221]	475	287.5

No.	TextName	CX	CY
401	G[222]	450	406.5
402	G[223]	425	287.5
403	G[224]	400	406.5
404	G[225]	375	287.5
405	G[226]	350	406.5
406	G[227]	325	287.5
407	G[228]	300	406.5
408	G[229]	275	287.5
409	G[230]	250	406.5
410	G[231]	225	287.5
411	G[232]	200	406.5
412	G[233]	175	287.5
413	G[234]	150	406.5
414	G[235]	125	287.5
415	G[236]	100	406.5
416	G[237]	75	287.5
417	G[238]	50	406.5
418	G[239]	25	287.5
419	G[240]	0	406.5
420	G[241]	-25	287.5
421	G[242]	-50	406.5
422	G[243]	-75	287.5
423	G[244]	-100	406.5
424	G[245]	-125	287.5
425	G[246]	-150	406.5
426	G[247]	-175	287.5
427	G[248]	-200	406.5
428	G[249]	-225	287.5
429	G[250]	-250	406.5
430	G[251]	-275	287.5
431	G[252]	-300	406.5
432	G[253]	-325	287.5
433	G[254]	-350	406.5
434	G[255]	-375	287.5
435	G[256]	-400	406.5
436	G[257]	-425	287.5
437	G[258]	-450	406.5
438	G[259]	-475	287.5
439	G[260]	-500	406.5
440	G[261]	-525	287.5

No.	TextName	CX	CY
441	G[262]	-550	406.5
442	G[263]	-575	287.5
443	G[264]	-600	406.5
444	G[265]	-625	287.5
445	G[266]	-650	406.5
446	G[267]	-675	287.5
447	G[268]	-700	406.5
448	G[269]	-725	287.5
449	G[270]	-750	406.5
450	G[271]	-775	287.5
451	G[272]	-800	406.5
452	G[273]	-825	287.5
453	G[274]	-850	406.5
454	G[275]	-875	287.5
455	G[276]	-900	406.5
456	G[277]	-925	287.5
457	G[278]	-950	406.5
458	G[279]	-975	287.5
459	G[280]	-1000	406.5
460	G[281]	-1025	287.5
461	G[282]	-1050	406.5
462	G[283]	-1075	287.5
463	G[284]	-1100	406.5
464	G[285]	-1125	287.5
465	G[286]	-1150	406.5
466	G[287]	-1175	287.5
467	G[288]	-1200	406.5
468	G[289]	-1225	287.5
469	G[290]	-1250	406.5
470	G[291]	-1275	287.5
471	G[292]	-1300	406.5
472	G[293]	-1325	287.5
473	G[294]	-1350	406.5
474	G[295]	-1375	287.5
475	G[296]	-1400	406.5
476	G[297]	-1425	287.5
477	G[298]	-1450	406.5
478	G[299]	-1475	287.5
479	G[300]	-1500	406.5
480	G[301]	-1525	287.5

No.	TextName	CX	CY
481	G[302]	-1550	406.5
482	G[303]	-1575	287.5
483	G[304]	-1600	406.5
484	G[305]	-1625	287.5
485	G[306]	-1650	406.5
486	G[307]	-1675	287.5
487	G[308]	-1700	406.5
488	G[309]	-1725	287.5
489	G[310]	-1750	406.5
490	G[311]	-1775	287.5
491	G[312]	-1800	406.5
492	G[313]	-1825	287.5
493	G[314]	-1850	406.5
494	G[315]	-1875	287.5
495	G[316]	-1900	406.5
496	G[317]	-1925	287.5
497	G[318]	-1950	406.5
498	G[319]	-1975	287.5
499	G[320]	-2000	406.5
500	G[321]	-2025	287.5
501	G[322]	-2050	406.5
502	G[323]	-2075	287.5
503	G[324]	-2100	406.5
504	G[325]	-2125	287.5
505	G[326]	-2150	406.5
506	G[327]	-2175	287.5
507	G[328]	-2200	406.5
508	G[329]	-2225	287.5
509	G[330]	-2250	406.5
510	G[331]	-2275	287.5
511	G[332]	-2300	406.5
512	G[333]	-2325	287.5
513	G[334]	-2350	406.5
514	G[335]	-2375	287.5
515	G[336]	-2400	406.5
516	G[337]	-2425	287.5
517	G[338]	-2450	406.5
518	G[339]	-2475	287.5
519	G[340]	-2500	406.5
520	G[341]	-2525	287.5

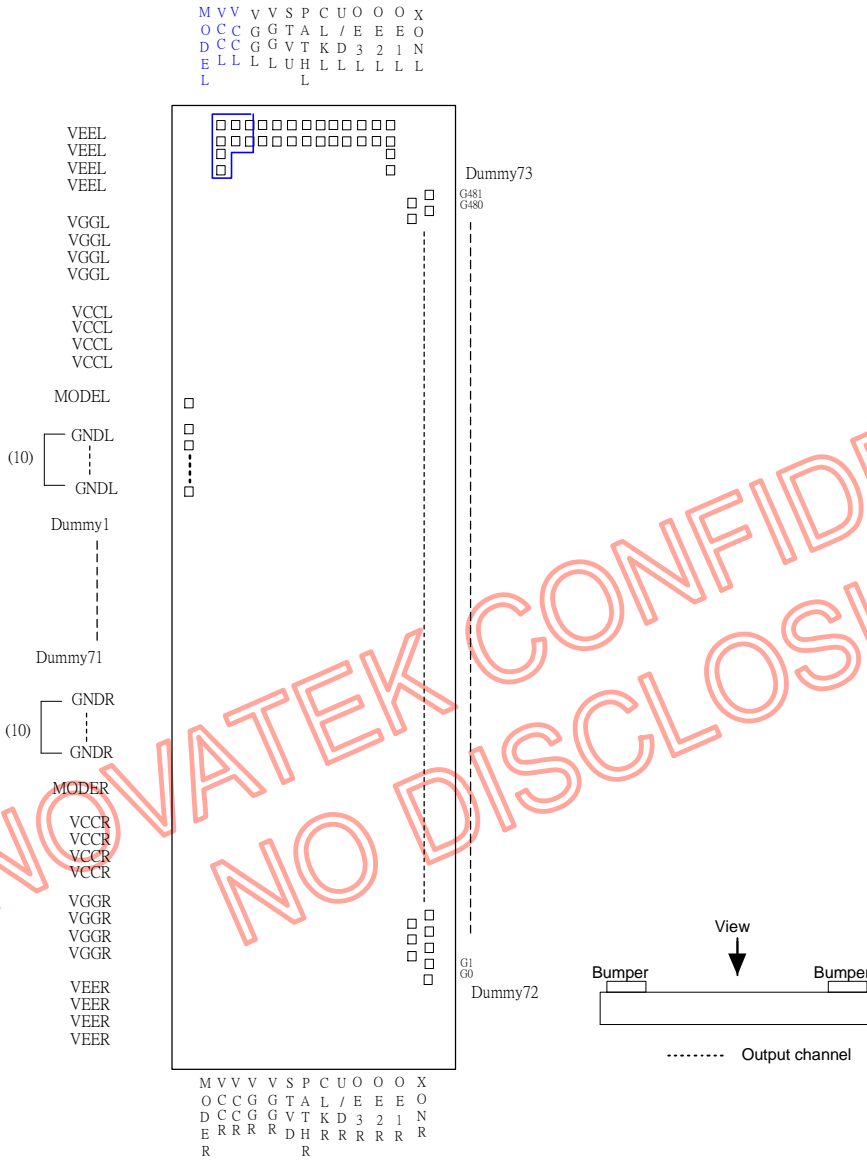
No.	TextName	CX	CY
521	G[342]	-2550	406.5
522	G[343]	-2575	287.5
523	G[344]	-2600	406.5
524	G[345]	-2625	287.5
525	G[346]	-2650	406.5
526	G[347]	-2675	287.5
527	G[348]	-2700	406.5
528	G[349]	-2725	287.5
529	G[350]	-2750	406.5
530	G[351]	-2775	287.5
531	G[352]	-2800	406.5
532	G[353]	-2825	287.5
533	G[354]	-2850	406.5
534	G[355]	-2875	287.5
535	G[356]	-2900	406.5
536	G[357]	-2925	287.5
537	G[358]	-2950	406.5
538	G[359]	-2975	287.5
539	G[360]	-3000	406.5
540	G[361]	-3025	287.5
541	G[362]	-3050	406.5
542	G[363]	-3075	287.5
543	G[364]	-3100	406.5
544	G[365]	-3125	287.5
545	G[366]	-3150	406.5
546	G[367]	-3175	287.5
547	G[368]	-3200	406.5
548	G[369]	-3225	287.5
549	G[370]	-3250	406.5
550	G[371]	-3275	287.5
551	G[372]	-3300	406.5
552	G[373]	-3325	287.5
553	G[374]	-3350	406.5
554	G[375]	-3375	287.5
555	G[376]	-3400	406.5
556	G[377]	-3425	287.5
557	G[378]	-3450	406.5
558	G[379]	-3475	287.5
559	G[380]	-3500	406.5
560	G[381]	-3525	287.5

No.	TextName	CX	CY
561	G[382]	-3550	406.5
562	G[383]	-3575	287.5
563	G[384]	-3600	406.5
564	G[385]	-3625	287.5
565	G[386]	-3650	406.5
566	G[387]	-3675	287.5
567	G[388]	-3700	406.5
568	G[389]	-3725	287.5
569	G[390]	-3750	406.5
570	G[391]	-3775	287.5
571	G[392]	-3800	406.5
572	G[393]	-3825	287.5
573	G[394]	-3850	406.5
574	G[395]	-3875	287.5
575	G[396]	-3900	406.5
576	G[397]	-3925	287.5
577	G[398]	-3950	406.5
578	G[399]	-3975	287.5
579	G[400]	-4000	406.5
580	G[401]	-4025	287.5
581	G[402]	-4050	406.5
582	G[403]	-4075	287.5
583	G[404]	-4100	406.5
584	G[405]	-4125	287.5
585	G[406]	-4150	406.5
586	G[407]	-4175	287.5
587	G[408]	-4200	406.5
588	G[409]	-4225	287.5
589	G[410]	-4250	406.5
590	G[411]	-4275	287.5
591	G[412]	-4300	406.5
592	G[413]	-4325	287.5
593	G[414]	-4350	406.5
594	G[415]	-4375	287.5
595	G[416]	-4400	406.5
596	G[417]	-4425	287.5
597	G[418]	-4450	406.5
598	G[419]	-4475	287.5
599	G[420]	-4500	406.5
600	G[421]	-4525	287.5

No.	TextName	CX	CY	No.	TextName	CX	CY
601	G[422]	-4550	406.5	641	G[462]	-5550	406.5
602	G[423]	-4575	287.5	642	G[463]	-5575	287.5
603	G[424]	-4600	406.5	643	G[464]	-5600	406.5
604	G[425]	-4625	287.5	644	G[465]	-5625	287.5
605	G[426]	-4650	406.5	645	G[466]	-5650	406.5
606	G[427]	-4675	287.5	646	G[467]	-5675	287.5
607	G[428]	-4700	406.5	647	G[468]	-5700	406.5
608	G[429]	-4725	287.5	648	G[469]	-5725	287.5
609	G[430]	-4750	406.5	649	G[470]	-5750	406.5
610	G[431]	-4775	287.5	650	G[471]	-5775	287.5
611	G[432]	-4800	406.5	651	G[472]	-5800	406.5
612	G[433]	-4825	287.5	652	G[473]	-5825	287.5
613	G[434]	-4850	406.5	653	G[474]	-5850	406.5
614	G[435]	-4875	287.5	654	G[475]	-5875	287.5
615	G[436]	-4900	406.5	655	G[476]	-5900	406.5
616	G[437]	-4925	287.5	656	G[477]	-5925	287.5
617	G[438]	-4950	406.5	657	G[478]	-5950	406.5
618	G[439]	-4975	287.5	658	G[479]	-5975	287.5
619	G[440]	-5000	406.5	659	G[480]	-6000	406.5
620	G[441]	-5025	287.5	660	G[481]	-6025	287.5
621	G[442]	-5050	406.5	661	DUMMY[73]	-6050	406.5
622	G[443]	-5075	287.5				
623	G[444]	-5100	406.5				
624	G[445]	-5125	287.5				
625	G[446]	-5150	406.5				
626	G[447]	-5175	287.5				
627	G[448]	-5200	406.5				
628	G[449]	-5225	287.5				
629	G[450]	-5250	406.5				
630	G[451]	-5275	287.5				
631	G[452]	-5300	406.5				
632	G[453]	-5325	287.5				
633	G[454]	-5350	406.5				
634	G[455]	-5375	287.5				
635	G[456]	-5400	406.5				
636	G[457]	-5425	287.5				
637	G[458]	-5450	406.5				
638	G[459]	-5475	287.5				
639	G[460]	-5500	406.5				
640	G[461]	-5525	287.5				

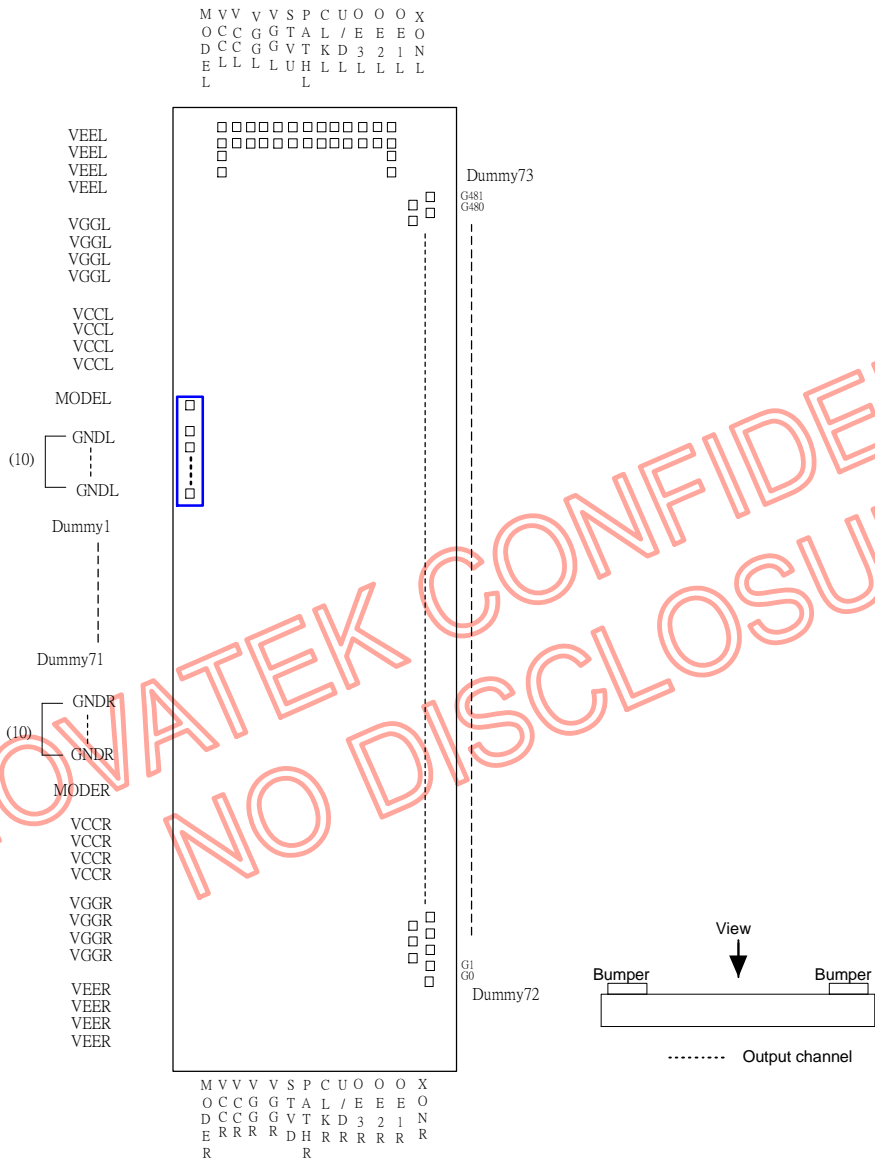
Application Notes

1. MODE = "H", channel number =480 (MODE pin connect to VCC)



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NO DISCLOSURE

2. MODE = "L", channel number =320 (MODE pin connect to GND)



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