ALL SHORE INDUSTRIES

ASI-O-270JAWWH70/M

No.	Items:	Specification:	Unit
1	Diagonal Size	2.70	Inch
2	Resolution	256(H) x 64(V)	Lines
3	Active Area	66.53 (W) x 16.61(H)	mm
4	Outline Dimension (Panel)	82.00 (W) x 25.50(H)	mm
5	Pixel Pitch	0.26 (W) x 0.26(H)	mm
6	Pixel Size	0.23 (W) x 0.23 (H)	mm
7	Driver IC	SSD1322UR1	-
8	Grayscale	4	Bit
9	Interface	Parallel / Serial	-
10	IC package type	COF with ZIF tail	-
11	Thickness	1.5±0.1	mm
12	Weight	<6.5	g
13	Duty	1/64	-

PRODUCT CONTENTS

REVISION HISTORY

Rev.	Contents	Date
1.0	First Release	2011-03-16
1.1	Update ELECTRO-OPTICAL CHARACTERISTICS Update EXTERNAL DIMENSIONS Update OUTGOING QUALITY CONTROL SPECIFICATION	2011-05-25
1.2	Update Life Time	2012-12-19

■ SERIES PRODUCTS LIST

Module	Display Color	CIE		Luminance typical(cd/m^2)	Lifetime (hrs@25℃)	
		x	y		30% ON*	100% ON*
	Red	0.65±0.04	0.34±0.04	30	150K	45K
				50	75K	22K
	Yellow	0.46±0.05	0.51±0.05	60	150K	45K
				100	70K	21K
	Green	0.31±0.04	0.62±0.04	80	80K	24K
				100	55K	16K
	Blue	0.16±0.05	0.27±0.05	60	80K	24K
				80	60K	18K
	White	0.3±0.05	0.36±0.05	60	80K	24K
				80	60K	18K

*30% ON:30% pixels scrolling display on;100% ON:All pixels display on

1、 **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	2.70	Inch
2	Resolution	256(H) x 64(V)	Lines
3	Active Area	66.53 (W) x 16.61(H)	mm
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9	Interface	Parallel / Serial	-
10	IC package type	COF with ZIF tail	-
11	Thickness	1.5±0.1	mm
12	Weight	<6.5	g
13	Duty	1/64	-

■ ABSOLUTE MAXIMUM RATINGS

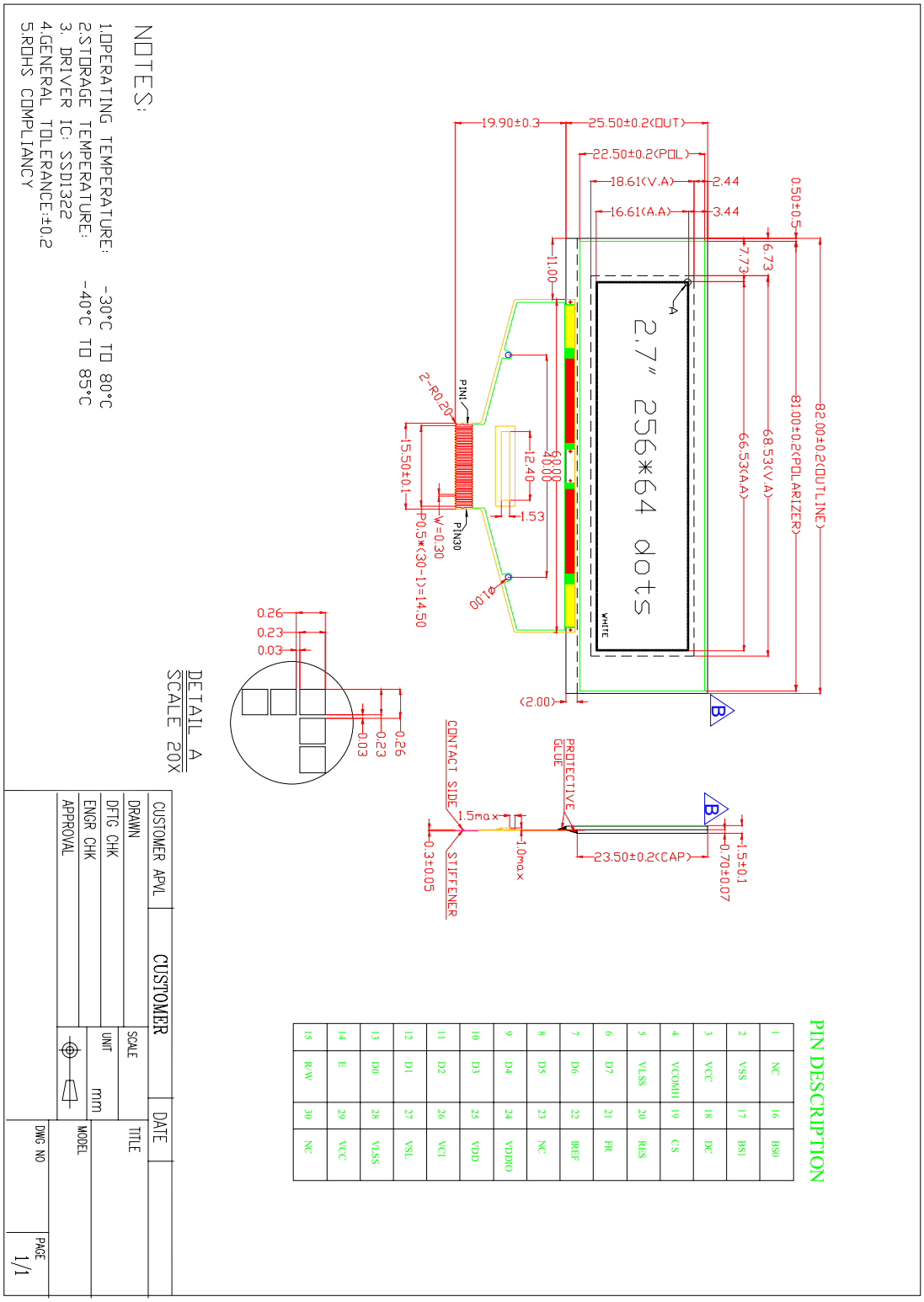
Unless otherwise specified, V_{SS} = 0V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	I/O	V_{DDIO}	-0.5	-	V_{CI}	V
	Logic	V_{CI}	-0.3	-	3.6	V
	Driving	V_{CC}	-0.5	-	21.0	V
	Core Logic	V_{DD}	-0.5	-	2.75	V
Operating Temperature		Top	-30	-	80	℃
Storage Temperature		Tst	-40	-	85	℃
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. **Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Unless otherwise specified, V_{SS} = 0V ,V_{CI}=2.4V to 3.5V. (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	I/O	V_{DDIO}	1.65	-	V_{CI}	V
	Logic	V_{CI}	2.4	3.0	3.5	V
	Operating	V_{CC}	10.0	14.0	20.0	V
	Core Logic	V_{DD}	2.4	-	2.6	
Input Voltage	High Voltage	V_{IH}	0.8 x V_{DDIO}	-	V_{DDIO}	V
	Low Voltage	V_{IL}	0	-	0.2 x V_{DDIO}	V
Output Voltage	High Voltage	V_{OH}	0.9x V_{DDIO}	-	V_{DDIO}	V
	Low Voltage	V_{OL}	0	-	0.1 x V_{DDIO}	V

◆POWER CONSUMPTION

Unless otherwise specified,VSS=0V,VDD=3.0V,Frame Frequency=100Hz

Module	VPP (V)	Contrast Command Set(hex)	Luminance (cd/m2)			Typical Power Consumption(mW)		Sleep Mode
			Min	Typical	Max	All pixels ON	30% pixels ON	
RED	9.5	0x3F	25	30	-	220	80	<5uA
YELLOW	9.5	0x3F	50	60	-	220	80	<5uA
GREEN	9.5	0x3F	70	80	-	230	90	<5uA
BLUE	12.0	0x3F	50	60	-	380	150	<5uA
WHITE	12.0	0x3F	50	60	-	390	155	<5uA

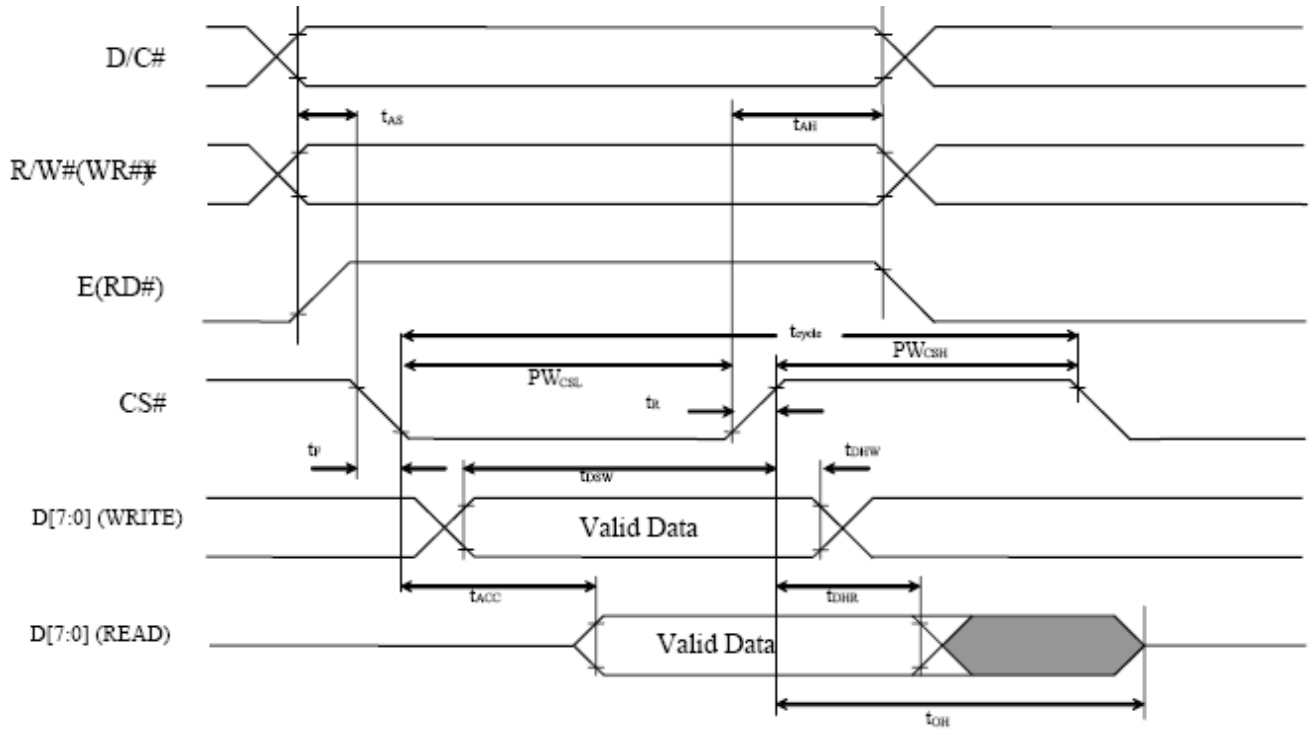
◆AC Characteristics

Use 8080/6800-Series MPU Parallel Interface or Serial Interface

1. 6800 Series MPU Parallel Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

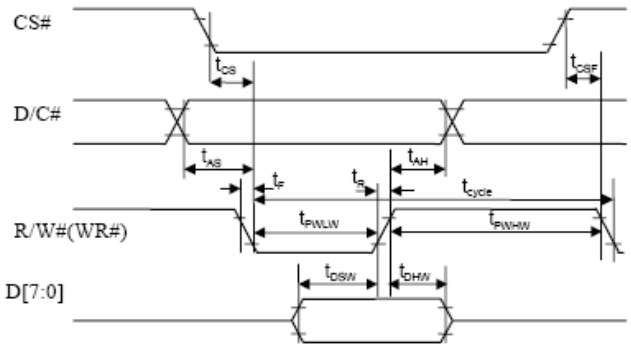


2. 8080 Series MPU Parallel Interface

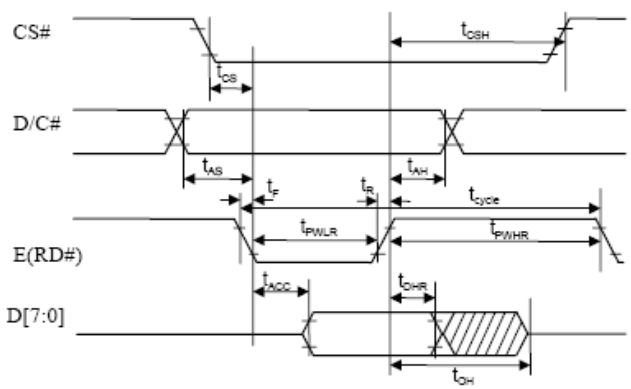
(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Write cycle



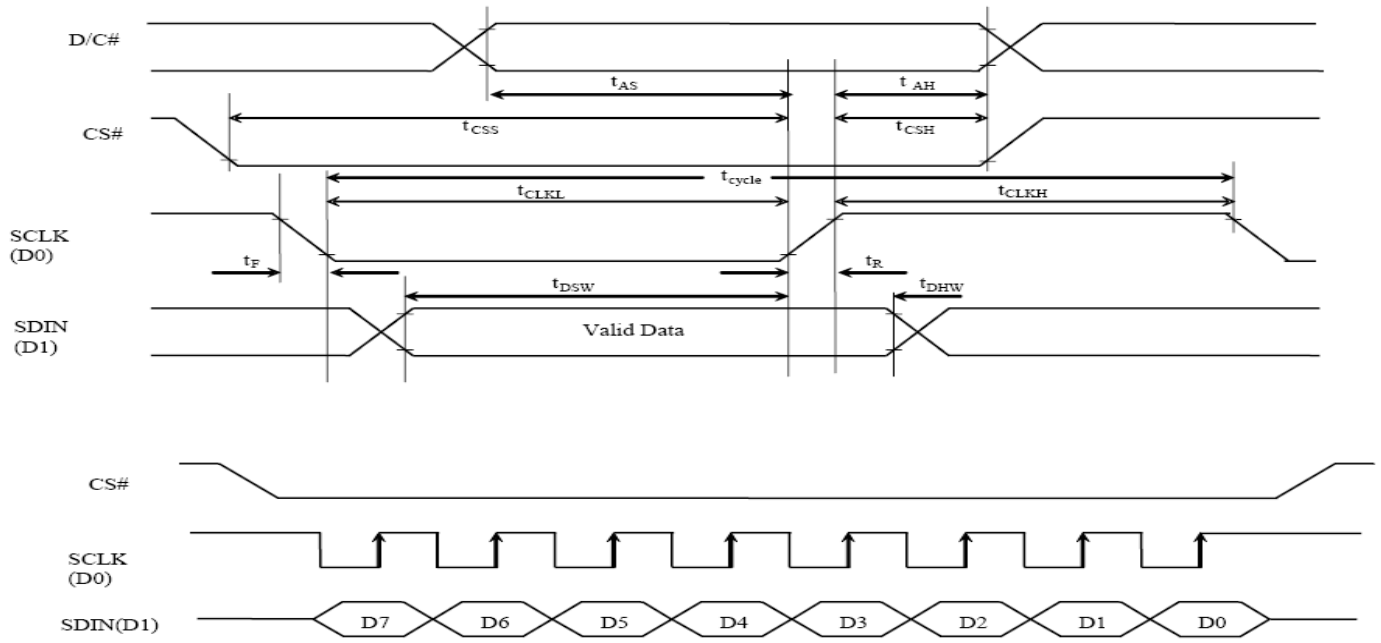
Read cycle



3. 4-Wire Serial Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

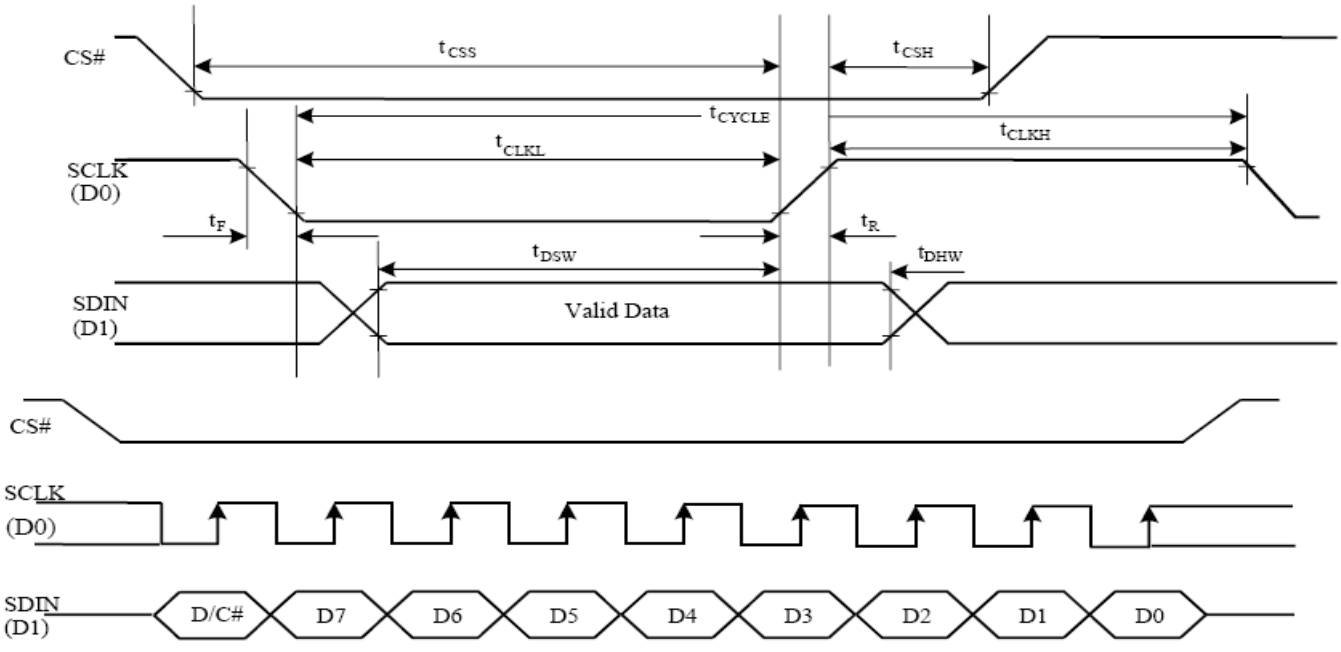
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



4. 3-Wire Serial Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

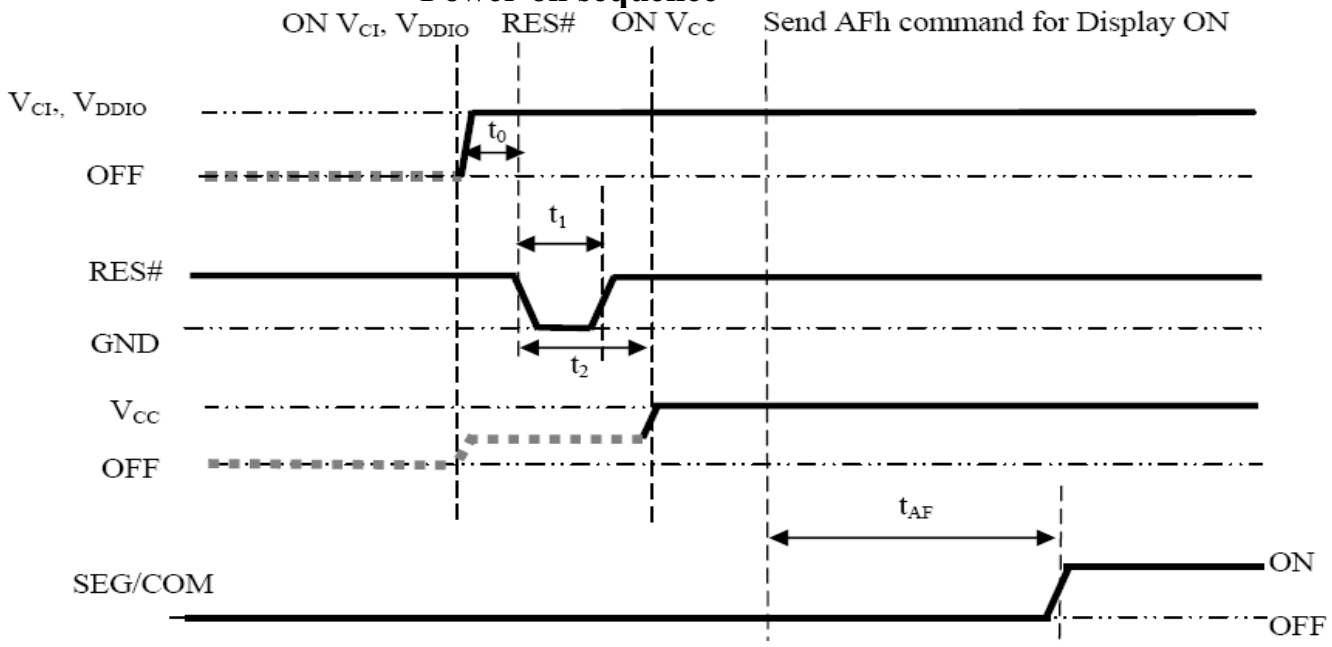


5. TIMING OF POWER SUPPLY

◆*Power ON sequence*:

1. Power ON $V_{CI,}$ $V_{DDIO.}$
2. After V_{CI}, V_{DDIO} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES pin LOW (logic low) for at least 100us (t_1) [4] and then HIGH (logic high).
3. After set RES pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

Power on sequence



◆*Power OFF sequence*:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC.}$[1], [2], [3]
3. Wait for t_{OFF}. Power OFF $V_{CI,}$ V_{DDIO}.(where Minimum t_{OFF}=0ms (5), Typical t_{OFF}=100ms)

Note:

[1] Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever $V_{CI,}$ V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure above.

[2] V_{CC} should be kept float (disable) when it is OFF.

[3] Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

[5] VCI, V_{DDIO} should not be Power OFF before VCC Power OFF.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	90	100*	-	cd /m^2	White
Power Consumption		P	-	280	290	mW	30% pixels on L=100 cd/m^2
Frame Frequency		Fr	-	100	-	Hz	
Color Coordinate	White	CIE x	0.255	0.295	0.335	CIE1931	Darkroom
		CIE y	0.295	0.335	0.375		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio		Cr	10000:1	-	-		Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-
Operating Life Time		-	20,000	-	-	Hours	L=100cd/m^2

Note:

1. 100 cd/m^2 is based on V_{CI}=3.0V, V_{CC}=14.0V, contrast command setting 0xCF**.**

2. Contrast ratio is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (30% pixels scrolling display on)
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC	No connection
2	VSS	Ground. Common Voltage Reference Pin
3	VCC	Power supply for panel driving voltage. Segment voltage
4	VCOMH	COM signal deselected voltage level. High Level Voltage Output Of COM Signal
5	VLSS	Analog system ground pin. Voltage Supply
6-13	D7-D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode, D2 is pulled low in SPI mode).
14	E (RD)	MCU Interface Input pin, in 6800 parallel mode, it is used as enable signal, read/write operation is initiated when this pin is set high with chip selected. In 8080 parallel mode, this pin receives read signal, read operation is initiated when this is pulled low with chip selected. When SPI interface is selected, this pin must be connected to ground.
15	R/W(WR)	MCU Interface Input pin, in 6800 parallel mode, it is used as read/write selection input, read mode will be carried out when This pin is pulled high while write mode with this pin pulled low. In 8080 parallel mode, this pin will be write input, write operation is initiated when this is pulled low with chip selected. When SPI interface is selected, this pin must be connected to ground.
16-17	BS0-1	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. **BS[1:0]** / **Bus Interface Selection** 00 / 4 line SPI 01 / 3 line SPI 10 / 8-bit 8080 parallel 11 / 8-bit 6800 parallel
18	D/C	This pin is Data/Command control pin connected to the MCU. When the pin is pulled HIGH, the content at D 7:0 will be interpreted as data. When the pin is pulled LOW, the content at D 7:0 will be interpreted as command.
19	CS	This pin is the chip select input connected to the MCU. The chip is enabled for MCU communication only when CS is pulled LOW.
20	RES	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.

21	FR	This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.
22	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS to maintain the current around 10uA.
23	NC	No connection.
24	VDDIO	Power supply for interface logic level. It should be matched with the MCU interface voltage level.
25	VDD	Power supply pin for core logic operation. A capacitor is required to connect between this pin and VSS.
26	VCI	Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO.
27	VSL	This is segment voltage reference pin. When external VSL is used, connect with resistor and diode to ground
28	VLSS	Analog system ground pin.
29	VCC	Power supply for panel driving voltage. Segment Voltage
30	NC	No Connection.

■ COMMAND TABLE

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 63) **Note** (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 1 1	A8 A[6:0] B[6:0]	1 0 0	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	1 A_3 B_3	0 A_2 B_2	0 A_1 B_1	0 A_0 B_0	Enable Partial Display	This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0]
0	A9	1	0	1	0	1	0	0	1	Exit Partial Display	This command is sent to exit the Partial Display mode
0 1	AB A[0]	1 0	0 0	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection	A[0]=0b, Select external V_{DD} A[0]=1b, Enable internal V_{DD} regulator [reset]
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:

A[3:0]	Phase 1 period
0000	invalid
0001	invalid
0010	5 DCLKs
0011	7 DCLKs
0100	9 DCLKs [reset]
:	:
1111	31 DCLKs

A[7:4]	Phase 2 period
0000	invalid
0001	invalid
0010	invalid
0011	3 DCLKs
:	:
0111	7 DCLKs [reset]
:	:
1111	15 DCLKs

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=0101b]</td></tr>
<tr><td>0
1
1</td><td>B4
A[1:0]
B[7:3]</td><td>1
1
B_7</td><td>0
0
B_6</td><td>1
1
B_5</td><td>1
0
B_4</td><td>0
0
B_3</td><td>1
0
1</td><td>0
A_1
0</td><td>0
A_0
1</td><td>Display Enhancement A</td><td>A[1:0] = 00b: Enable external VSL
A[1:0] = 10b: Internal VSL [reset]

B[7:3] = 11111b: Enhanced low GS display quality
B[7:3] = 10110b: Normal [reset]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
.....
1000b 8 dclks [reset]
.....
1111b 15 dclks</td></tr>
</table>

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15 Refer to Section 8.8 for details (2) The setting must be followed by the Enable Gray Scale Table command (00h)
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A14[7:0]	$A14_7$	$A14_6$	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
1	A15[7:0]	$A15_7$	$A15_6$	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112 Refer to Section 8.8 for details
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]
1	A[4:0]	*	*	*	A_4	A_3	A_2	A_1	A_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	Set COM deselect voltage level [reset = 04h]
1	A[2:0]	*	*	*	*	0	A_2	A_1	A_0		
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current	A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I_{SEG} current [reset = 7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[4:0]	Hex code	pre-charge voltage
00000	00h	0.20 x V_{CC}
:	:	:
11111	1Fh	0.60 x V_{CC}

A[2:0]	Hex code	V_{COMH}
000	00h	0.72 x V_{CC}
:	:	:
100	04h	0.80 x V_{CC} [reset]
:	:	:
111	07h	0.86 x V_{CC}

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset]
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset]
1	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	D1	1	1	0	1	0	0	0	1	Display Enhancement B	
1	A[5:4]	1	0	A_5	A_4	0	0	1	0		A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
1	20	0	0	1	0	0	0	0	0		
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
1	A[2]	0	0	0	1	0	A_2	1	0		

■ INITIALIZATION CODE

```
void Inital_SSD1322()
{
  WMLCDCOM(0xFD);//Command lock setting
  WMLCDDATA(0x12);

  WMLCDCOM(0xAE);//Display OFF

  WMLCDCOM(0x15);//column address setting
  WMLCDDATA(0x1C);
  WMLCDDATA(0x5B);

  WMLCDCOM(0x75);//row address setting
  WMLCDDATA(0x00);
  WMLCDDATA(0x3F);

  WMLCDCOM(0xA0);//re_map&dual com mode
  WMLCDDATA(0x14);
  WMLCDDATA(0x11);//enable dual com mode

  WMLCDCOM(0xA1);//display start line
  WMLCDDATA(0x00);

  WMLCDCOM(0xA2);//display offset
  WMLCDDATA(0x00);

  WMLCDCOM(0xA6);//normal display

  //WMLCDCOM(0xA8);//partial display setting
  //WMLCDDATA(0x00);//start row
  //WMLCDDATA(0x3F);//end row

  //WMLCDCOM(0xA9);//exit partial display mode

  WMLCDCOM(0xAB);//function selection
  WMLCDDATA(0x01);//enable internal vdd

  WMLCDCOM(0xB1);//phase length setting
  WMLCDDATA(0x74);//phase1=9dclk.phase2=7dclk
```

```
WMLCDCOM(0xB3);//front clock divider&oscillator freq
WMLCDDATA(0x51);

WMLCDCOM(0xB4);//display enhancement A
WMLCDDATA(0xA2);//INTERNAL VSL
WMLCDDATA(0xB5);//normal or 11111101 to enhance low GS

//WMLCDCOM(0xB5);//GPIO SETTING
//WMLCDDATA(0x0a);

WMLCDCOM(0xB6);//second precharge period setting
WMLCDDATA(0x08);

WMLCDCOM(0xBB);//set precharge voltage
WMLCDDATA(0x17);

WMLCDCOM(0xBE);//set VCOMH voltage
WMLCDDATA(0x04);//0.80*VCC

WMLCDCOM(0xC1);//contrast set
WMLCDDATA(CONTRAST);

WMLCDCOM(0xC7);//master current set
WMLCDDATA(0x0F);

WMLCDCOM(0xCA);//mux set
WMLCDDATA(0x3F);

WMLCDCOM(0xD1);//display enhancement B
WMLCDDATA(0xA2);
WMLCDDATA(0x20);

WMLCDCOM(0x00);//enable gray scale setting
WMLCDCOM(0xB8);//gray scale setting
WMLCDDATA(0x00);//GS1=0
WMLCDDATA(0x0C);//GS2=8
WMLCDDATA(0x18);//GS3=8
WMLCDDATA(0x24);//GS4=8
WMLCDDATA(0x30);//GS5=9
WMLCDDATA(0x3C);//GS6=9
```

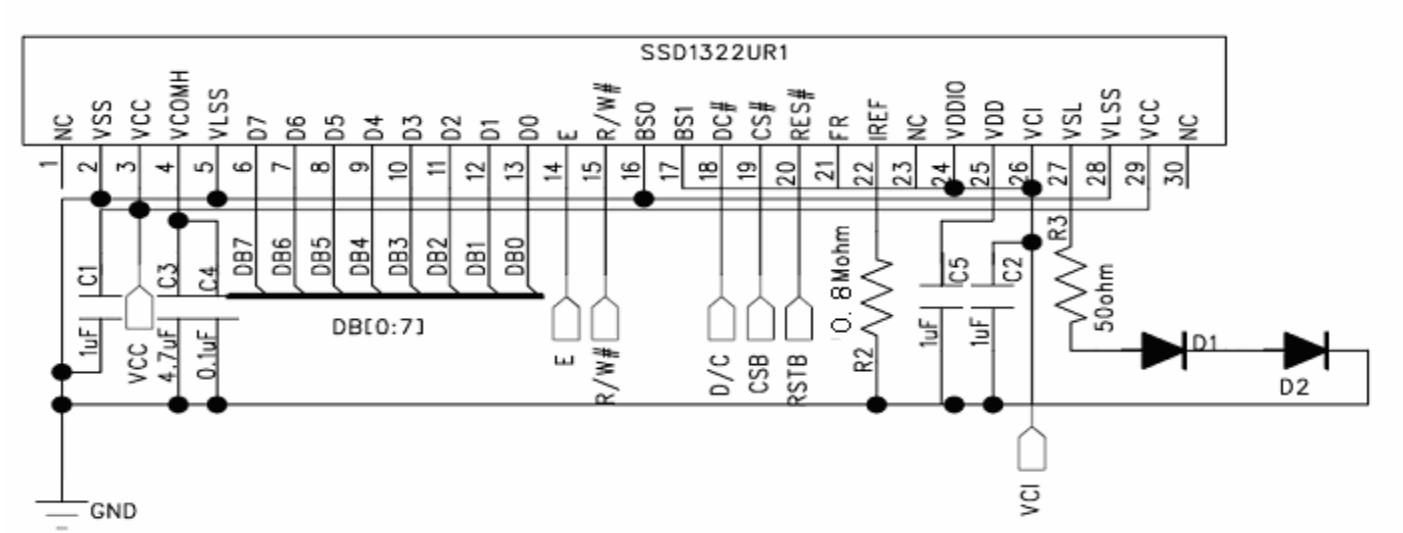
```
  WMLCDDATA(0x48);//GS7=9
  WMLCDDATA(0x54);//GS8=10
  WMLCDDATA(0x60);//GS9=10
  WMLCDDATA(0x6C);//GS10=10
  WMLCDDATA(0x78);//GS11=10
  WMLCDDATA(0x84);//GS12=10
  WMLCDDATA(0x90);//GS13=11
  WMLCDDATA(0x9C);//GS14=11
  WMLCDDATA(0xA8);//GS15=12

  WMLCDCOM(0xAF);//Display ON

}
```

Note:

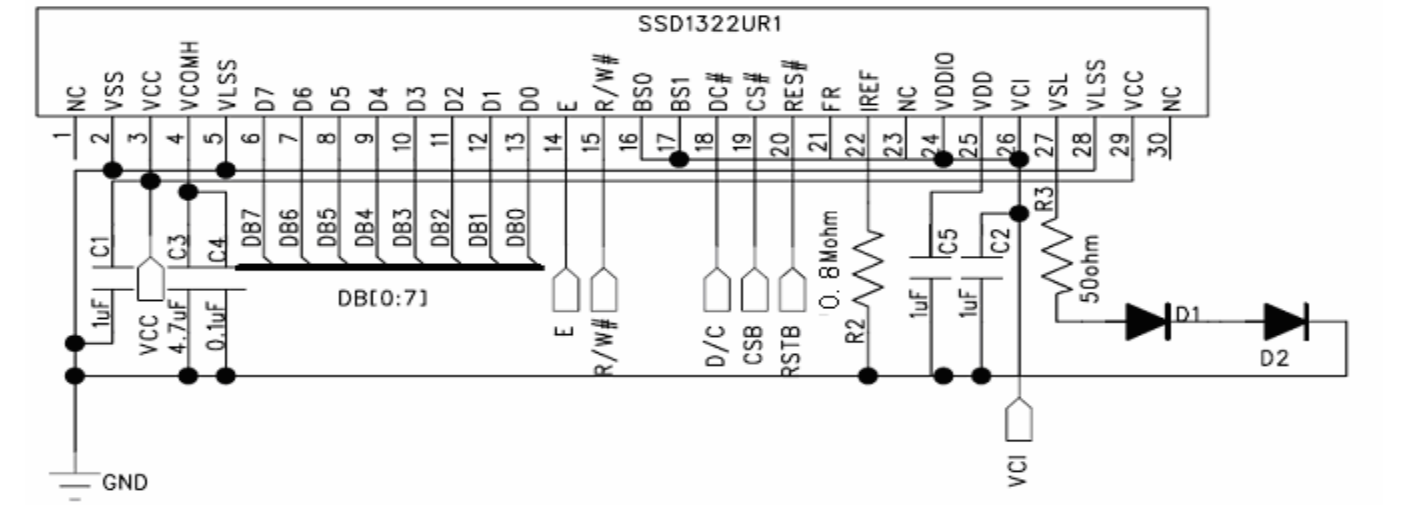
Set appropriate parameters of initialization base on actual application.

■ SCHEMATIC EXAMPLE

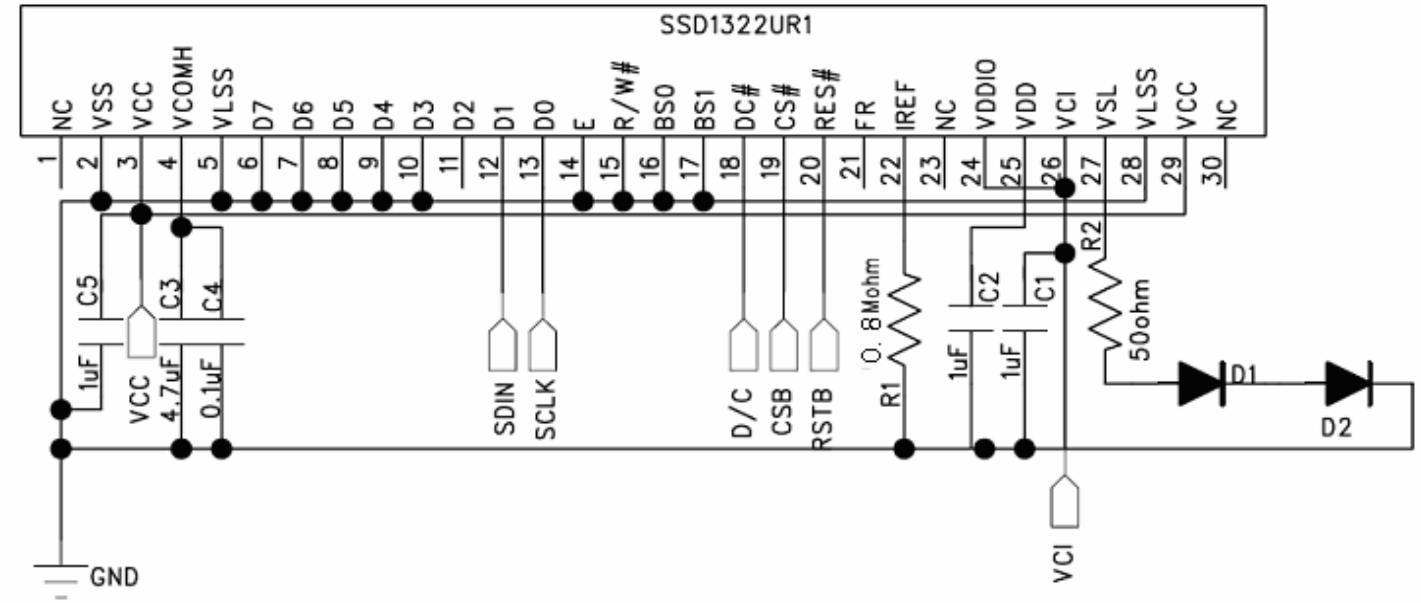
◆8080 Series Interface Application Circuit(External V_{CC}=14.0V):



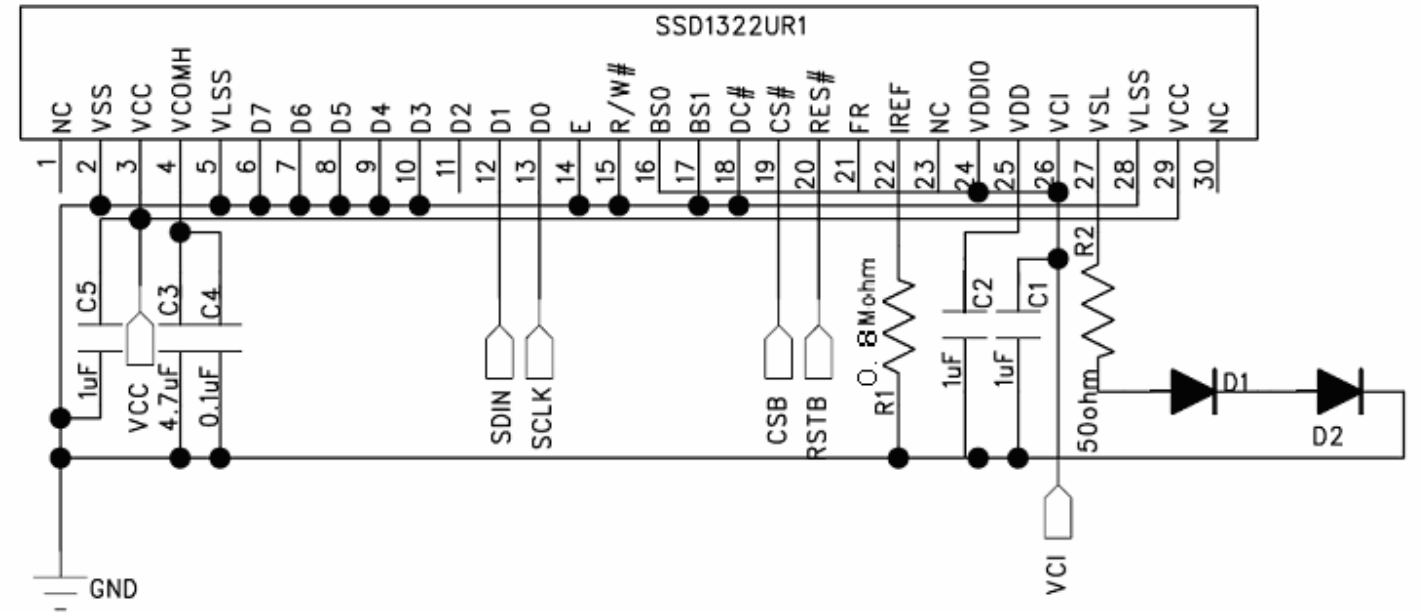
◆6800 Series Interface Application Circuit(External V_{CC}=14.0V):



◆4-wire SPI Interface Application Circuit(External V_{CC}=14.0V):



◆3-wire SPI Interface Application Circuit(External V_{CC}=14.0V):



NOTE:

Voltage at IREF = VCC – 6V. For VCC = 14V, IREF = 10uA :

R1 = (Voltage at IREF - VSS) / IREF= (14 - 6) / 10u= 0.8MΩ

R2 = 50Ω, 1/8W (1)

D1 - D2 = Vth = 0.7V, 1N4148 (1)

C1 ~ C2, C3, C5: 4.7uF, C4: 0.1uF

Note

(1) The value is recommended value. Select appropriate value against module application.

■ RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage
(HTS)</td><td>80±2℃, 200 hours</td><td rowspan="6">1. After testing, the function test is ok.
2. After testing, no addition to the defect.
3. After testing, the change of luminance should be within +/- 50% of initial value.
4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.
5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating
(HTO)</td><td>70±2℃, 96 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage
(LTS)</td><td>-30±2℃, 200 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating
(LTO)</td><td>-20±2℃, 96 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage
(HTHHS)</td><td>50±3℃, 90%±3%RH, 120 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation)
(TS)</td><td>-20±2℃ ~ 25℃ ~ 70±2℃
(30min) (5min) (30min)
10cycles</td></tr>
<tr><td>Vibration (Packing)</td><td>10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z</td><td colspan="2" rowspan="2">1. One box for each test.
2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop (Packing)</td><td>Height : 1 m, each time for 6 sides, 3 edges, 1 angle</td></tr>
<tr><td>ESD (finished product housing)</td><td>±4kV (R: 330Ω C: 150pF , 10times, air discharge)</td><td colspan="2">1. After testing, cosmetic and electrical defects should not happen.
2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.</td></tr>
</table>

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

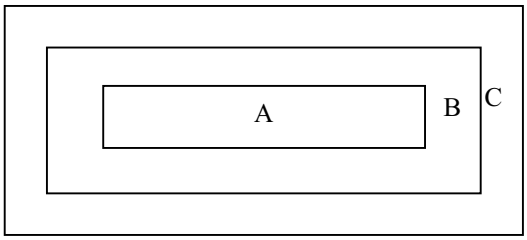
■ OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

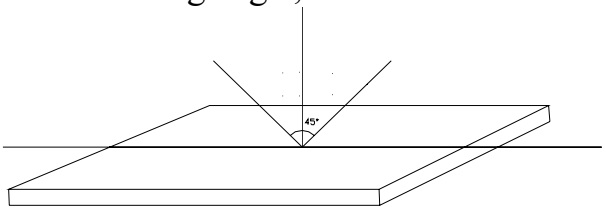
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



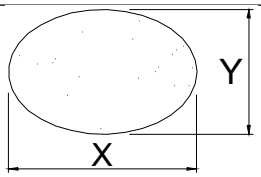
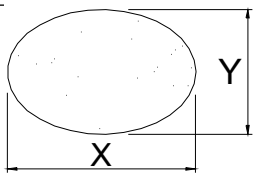
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

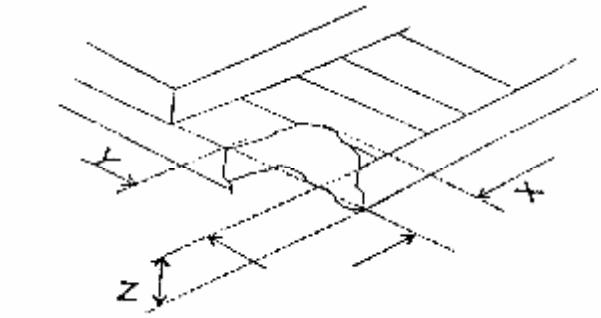
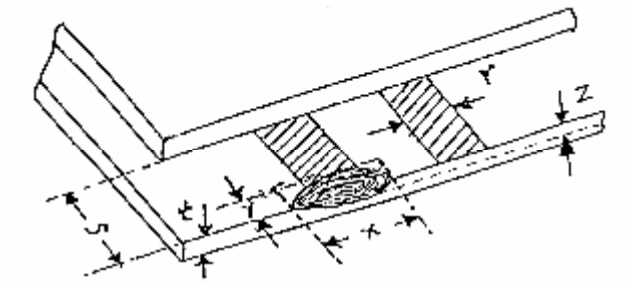
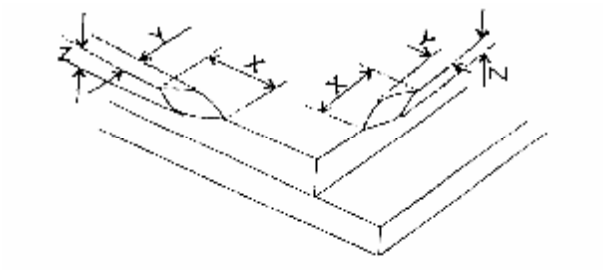
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td>0.15＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="6">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness s: pad width a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) All Shore will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with All Shore OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to All Shore within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of All Shore is limited to repair and/or replacement on the terms above. All Shore will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For All Shore standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.